# PIC10(L)F320/322

6/8-Pin Flash-Based, 8-Bit Microcontrollers

## High-Performance RISC CPU
- **Only 35 Instructions to Learn:**
  - All single-cycle instructions, except branches
- **Operating Speed:**
  - DC – 16 MHz clock input
  - DC – 250 ns instruction cycle
- **Eight-level Deep Hardware Stack**
- **Interrupt Capability**
- **Processor Self-Write/Read access to Program Memory**
- **Pinout Compatible to other 6-Pin PIC10FXXX Microcontrollers**

## Memory
- **Up to 512 Words of Flash Program Memory**
- **64 Bytes Data Memory**
- **High-Endurance Flash Data Memory (HEF)**
  - 128B of nonvolatile data storage
  - 100K erase/write cycles

## Special Microcontroller Features
- **Low-Power 16 MHz Internal Oscillator:**
  - Software selectable frequency range from 16 MHz to 31 kHz
  - Factory calibrated to ±1%, typical
- **Wide Operating Range:**
  - 1.8V to 3.6V (PIC10LF320/322)
  - 2.3V to 5.5V (PIC10F320/322)
- **Power-On Reset (POR)**
- **Power-up Timer (PWRT)**
- **Brown-Out Reset (BOR)**
- **Ultra Low-Power Sleep Regulator**
- **Extended Watchdog Timer (WDT)**
- **Programmable Code Protection**
- **Power-Saving Sleep mode**
- **Selectable Oscillator Options (EC mode or Internal Oscillator)**
- **In-Circuit Serial Programming™ (ICSP™) (via Two Pins)**
- **In-Circuit Debugger Support**
- **Fixed Voltage Reference (FVR) with 1.024V, 2.048V and 4.096V (‘F’ variant only) Output Levels**
- **Integrated Temperature Indicator**
- **40-year Flash Data Retention**

## eXtreme Low-Power (XLP) Features (PIC10LF320/322)
- **Sleep Current:**
  - 20 nA @ 1.8V, typical
- **Operating Current:**
  - 25 μA @ 1 MHz, 1.8V, typical
- **Watchdog Timer Current:**
  - 500 nA @ 1.8V, typical

## Peripheral Features
- **Four I/O Pins:**
  - One input-only pin
  - High current sink/source for LED drivers
  - Individually selectable weak pull-ups
  - Interrupt-on-Change
- **Timer0:** 8-Bit Timer/Counter with 8-Bit Programmable Prescaler
- **Timer2:** 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler
- **Two PWM modules:**
  - 10-bit PWM, max. frequency 16 kHz
  - Combined to single 2-phase output
- **A/D Converter:**
  - 8-bit resolution with 3 channels
- **Configurable Logic Cell (CLC):**
  - 8 selectable input source signals
  - Two inputs per module
  - Software selectable logic functions including:
    - AND/OR/XOR/D Flop/D Latch/SR/JK
    - External or internal inputs/outputs
  - Operation while in Sleep
- **Numerically Controlled Oscillator (NCO):**
  - 20-bit accumulator
  - 16-bit increment
  - Linear frequency control
  - High-speed clock input
  - Selectable Output modes
    - Fixed Duty Cycle (FDC)
    - Pulse Frequency (PF) mode
- **Complementary Waveform Generator (CWG):**
  - Selectable falling and rising edge dead-band control
  - Polarity control
  - Two auto-shutdown sources
  - Multiple input sources: PWM, CLC, NCO
## PIC10(L)F320/322 Family Types

<table>
<thead>
<tr>
<th>Device</th>
<th>Data Sheet Index</th>
<th>Data Sheet Memory</th>
<th>Program Memory Flash (words)</th>
<th>Flash (bytes)</th>
<th>Data SRAM (bytes)</th>
<th>High Endurance Flash (bytes)</th>
<th>I/O’s(2)</th>
<th>8-Bit ADC (ch)</th>
<th>Timers (8-Bit)</th>
<th>PWM</th>
<th>Complementary Wave Generator (CWG)</th>
<th>Configurable Logic Cell (CLC)</th>
<th>Fixed Voltage Reference (FVR)</th>
<th>Numerically Controlled Oscillator (NCO)</th>
<th>Debug(1)</th>
<th>XLP</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC10(L)F320</td>
<td>(1)</td>
<td>256</td>
<td>64</td>
<td>128</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>H</td>
</tr>
<tr>
<td>PIC10(L)F322</td>
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<td>512</td>
<td>64</td>
<td>128</td>
<td>4</td>
<td>3</td>
<td>2</td>
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<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>H</td>
</tr>
</tbody>
</table>

**Note 1:**
- I - Debugging, Integrated on Chip; H - Debugging, Available using Debug Header;
- E - Emulation, Available using Emulation Header.
- One pin is input-only.

**Data Sheet Index:**
1: DS40001585 PIC10(L)F320/322 Data Sheet, 6/8 Pin High Performance, Flash Microcontrollers.

**Note:** For other small form-factor package availability and marking information, please visit [http://www.microchip.com/packaging](http://www.microchip.com/packaging) or contact your local sales office.
### FIGURE 1: 6-PIN DIAGRAM, PIC10(L)F320/322

<table>
<thead>
<tr>
<th>SOT-23</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICSPDAT/RA0</td>
</tr>
<tr>
<td>Vss</td>
</tr>
<tr>
<td>ICSPCLK/RA1</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>---</td>
</tr>
<tr>
<td>PIC10(L)F320</td>
</tr>
<tr>
<td>4</td>
</tr>
<tr>
<td>RA2</td>
</tr>
<tr>
<td>RA3/MCLR/Vpp</td>
</tr>
</tbody>
</table>

### FIGURE 2: 8-PIN DIAGRAM, PIC10(L)F320/322

<table>
<thead>
<tr>
<th>PDIP, DFN</th>
</tr>
</thead>
<tbody>
<tr>
<td>N/C</td>
</tr>
<tr>
<td>Vdd</td>
</tr>
<tr>
<td>RA2</td>
</tr>
<tr>
<td>ICSPCLK/RA1</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>---</td>
</tr>
<tr>
<td>PIC10(L)F320</td>
</tr>
<tr>
<td>RA3/MCLR/Vpp</td>
</tr>
<tr>
<td>Vss</td>
</tr>
<tr>
<td>N/C</td>
</tr>
<tr>
<td>RA0/ICSPDAT</td>
</tr>
</tbody>
</table>

### TABLE 1: 6 AND 8-PIN ALLOCATION TABLE, PIC10(L)F320/322

<table>
<thead>
<tr>
<th>I/O</th>
<th>6-Pin</th>
<th>8-Pin</th>
<th>Analog</th>
<th>Timer</th>
<th>PWM</th>
<th>Interrupts</th>
<th>Pull-ups</th>
<th>CWG</th>
<th>NCO</th>
<th>CLC</th>
<th>Basic</th>
<th>ICSP</th>
</tr>
</thead>
<tbody>
<tr>
<td>RA0</td>
<td>1</td>
<td>5</td>
<td>AN0</td>
<td>—</td>
<td>PWM1</td>
<td>IOC0</td>
<td>Y</td>
<td>CWG1A</td>
<td>—</td>
<td>CLC1IN0</td>
<td>—</td>
<td>ICSPDAT</td>
</tr>
<tr>
<td>RA1</td>
<td>3</td>
<td>4</td>
<td>AN1</td>
<td>—</td>
<td>PWM2</td>
<td>IOC1</td>
<td>Y</td>
<td>CWG1B</td>
<td>NCO1CLK</td>
<td>CLC1</td>
<td>CLKIN</td>
<td>ICSPCLK</td>
</tr>
<tr>
<td>RA2</td>
<td>4</td>
<td>3</td>
<td>AN2</td>
<td>T0CKI</td>
<td>—</td>
<td>INT/IOC2</td>
<td>Y</td>
<td>CWG1FLT</td>
<td>NCO1</td>
<td>CLC1IN1</td>
<td>CLKR</td>
<td></td>
</tr>
<tr>
<td>RA3</td>
<td>6</td>
<td>8</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>IOC3</td>
<td>Y</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>MCLR Vpp</td>
</tr>
<tr>
<td>N/C</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>N/C</td>
<td>—</td>
<td>6</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Vdd</td>
<td>5</td>
<td>2</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Vdd</td>
</tr>
<tr>
<td>Vss</td>
<td>2</td>
<td>7</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Vss</td>
</tr>
</tbody>
</table>
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1.0 DEVICE OVERVIEW

The PIC10(L)F320/322 are described within this data sheet. They are available in 6/8-pin packages. Figure 1-1 shows a block diagram of the PIC10(L)F320/322 devices. Table 1-2 shows the pinout descriptions.

Reference Table 1-1 for peripherals available per device.

### TABLE 1-1: DEVICE PERIPHERAL SUMMARY

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>PIC10(L)F320</th>
<th>PIC10(L)F322</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog-to-Digital Converter (ADC)</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>Configurable Logic Cell (CLC)</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>Complementary Wave Generator (CWG)</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>Fixed Voltage Reference (FVR)</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>Numerically Controlled Oscillator (NCO)</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>Temperature Indicator</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>PWM Modules</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PWM1</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>PWM2</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>Timers</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Timer0</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>Timer2</td>
<td>●</td>
<td>●</td>
</tr>
</tbody>
</table>
FIGURE 1-1: PIC10(L)F320/322 BLOCK DIAGRAM

Note 1: See applicable chapters for more information on peripherals.
## TABLE 1-2: PIC10(L)F320/322 PINOUT DESCRIPTION

<table>
<thead>
<tr>
<th>Name</th>
<th>Function</th>
<th>Input Type</th>
<th>Output Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RA0/PWM1/CLC1IN0/CWG1A/AN0/ICSPDAT</td>
<td>RA0</td>
<td>TTL</td>
<td>CMOS</td>
<td>General purpose I/O with IOC and WPU.</td>
</tr>
<tr>
<td>PWM1</td>
<td>—</td>
<td>CMOS</td>
<td>—</td>
<td>PWM output.</td>
</tr>
<tr>
<td>CLC1IN0</td>
<td>ST</td>
<td>—</td>
<td>CLC output.</td>
<td></td>
</tr>
<tr>
<td>CWG1A</td>
<td>—</td>
<td>CMOS</td>
<td>CWG primary output.</td>
<td></td>
</tr>
<tr>
<td>AN0</td>
<td>AN</td>
<td>—</td>
<td>A/D Channel input.</td>
<td></td>
</tr>
<tr>
<td>ICSPDAT</td>
<td>ST</td>
<td>CMOS</td>
<td>ICSP™ Data I/O.</td>
<td></td>
</tr>
<tr>
<td>RA1/PWM2/CLC1/CWG1B/AN1/CLKIN/ICSPCLK/NCO1CLK</td>
<td>RA1</td>
<td>TTL</td>
<td>CMOS</td>
<td>General purpose I/O with IOC and WPU.</td>
</tr>
<tr>
<td>PWM2</td>
<td>—</td>
<td>CMOS</td>
<td>—</td>
<td>PWM output.</td>
</tr>
<tr>
<td>CLC1</td>
<td>—</td>
<td>CMOS</td>
<td>—</td>
<td>CLC output.</td>
</tr>
<tr>
<td>CWG1B</td>
<td>—</td>
<td>CMOS</td>
<td>CWG complementary output.</td>
<td></td>
</tr>
<tr>
<td>AN1</td>
<td>AN</td>
<td>—</td>
<td>A/D Channel input.</td>
<td></td>
</tr>
<tr>
<td>CLKIN</td>
<td>ST</td>
<td>—</td>
<td>External Clock input (EC mode).</td>
<td></td>
</tr>
<tr>
<td>ICSPCLK</td>
<td>ST</td>
<td>—</td>
<td>ICSP™ Programming Clock.</td>
<td></td>
</tr>
<tr>
<td>NCO1CLK</td>
<td>ST</td>
<td>—</td>
<td>Numerical Controlled Oscillator external clock input.</td>
<td></td>
</tr>
<tr>
<td>RA2/INT/T0CKI/NCO1/CLC1IN1/CLKR/AN2/CWG1FLT</td>
<td>RA2</td>
<td>TTL</td>
<td>CMOS</td>
<td>General purpose I/O with IOC and WPU.</td>
</tr>
<tr>
<td>INT</td>
<td>ST</td>
<td>—</td>
<td>External interrupt.</td>
<td></td>
</tr>
<tr>
<td>T0CKI</td>
<td>ST</td>
<td>—</td>
<td>Timer0 clock input.</td>
<td></td>
</tr>
<tr>
<td>NCO1</td>
<td>—</td>
<td>CMOS</td>
<td>Numerically Controlled Oscillator output.</td>
<td></td>
</tr>
<tr>
<td>CLC1IN1</td>
<td>ST</td>
<td>—</td>
<td>CLC input.</td>
<td></td>
</tr>
<tr>
<td>CLKR</td>
<td>—</td>
<td>CMOS</td>
<td>Clock Reference output.</td>
<td></td>
</tr>
<tr>
<td>AN2</td>
<td>AN</td>
<td>—</td>
<td>A/D Channel input.</td>
<td></td>
</tr>
<tr>
<td>CWG1FLT</td>
<td>ST</td>
<td>—</td>
<td>Complementary Waveform Generator Fault 1 source input.</td>
<td></td>
</tr>
<tr>
<td>RA3/MCLR/VPP</td>
<td>RA3</td>
<td>TTL</td>
<td>—</td>
<td>General purpose input.</td>
</tr>
<tr>
<td>MCLR</td>
<td>ST</td>
<td>—</td>
<td>Master Clear with internal pull-up.</td>
<td></td>
</tr>
<tr>
<td>VPP</td>
<td>HV</td>
<td>—</td>
<td>Programming voltage.</td>
<td></td>
</tr>
<tr>
<td>VDD</td>
<td>VDD</td>
<td>Power</td>
<td>—</td>
<td>Positive supply.</td>
</tr>
<tr>
<td>VSS</td>
<td>VSS</td>
<td>Power</td>
<td>—</td>
<td>Ground reference.</td>
</tr>
</tbody>
</table>

**Legend:**
- **AN** = Analog input or output
- **CMOS** = CMOS compatible input or output
- **TTL** = CMOS input with TTL levels
- **ST** = CMOS input with Schmitt Trigger levels
- **HV** = High Voltage
2.0 MEMORY ORGANIZATION

These devices contain the following types of memory:

- Program Memory
  - Configuration Word
  - Device ID
  - User ID
  - Flash Program Memory

- Data Memory
  - Core Registers
  - Special Function Registers
  - General Purpose RAM
  - Common RAM

The following features are associated with access and control of program memory and data memory:

- PCL and PCLATH
- Stack
- Indirect Addressing

2.1 Program Memory Organization

The mid-range core has a 13-bit program counter capable of addressing 8K x 14 program memory space. This device family only implements up to 512 words of the 8K program memory space. Table 2-1 shows the memory sizes implemented for the PIC10(L)F320/322 family. Accessing a location above these boundaries will cause a wrap-around within the implemented memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figures 2-1, and 2-2).

<table>
<thead>
<tr>
<th>Device</th>
<th>Program Memory Space (Words)</th>
<th>Last Program Memory Address</th>
<th>High-Endurance Flash Memory Address Range (1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC10(L)F320</td>
<td>256</td>
<td>00FFh</td>
<td>0080h-00FFh</td>
</tr>
<tr>
<td>PIC10(L)F322</td>
<td>512</td>
<td>01FFh</td>
<td>0180h-01FFh</td>
</tr>
</tbody>
</table>

Note 1: High-endurance Flash applies to low byte of each address in the range.
FIGURE 2-1: PROGRAM MEMORY MAP AND STACK FOR PIC10(L)F320

PC<12:0>  
CALL, RETURN, RETLW, RETFIE  

Stack Level 0  
Stack Level 1  
Stack Level 8  

Reset Vector  
Interrupt Vector  
Page 0  
Rollover to Page 0  

On-chip Program Memory  

0000h  
0004h  
0005h  
00FFh  
0100h

FIGURE 2-2: PROGRAM MEMORY MAP AND STACK FOR PIC10(L)F322

PC<12:0>  
CALL, RETURN, RETLW, RETFIE  

Stack Level 0  
Stack Level 1  
Stack Level 8  

Reset Vector  
Interrupt Vector  
Page 0  
Rollover to Page 0  

On-chip Program Memory  

0000h  
0004h  
0005h  
01FFh  
0200h

Rollover to Page 0  

FFFh
2.2 Data Memory Organization

The data memory is in one bank, which contains the General Purpose Registers (GPR) and the Special Function Registers (SFR). The RP<1:0> bits of the STATUS register are the bank select bits.

RP1  RP0
0  0  → Bank 0 is selected

The bank extends up to 7Fh (128 bytes). The lower locations of the bank are reserved for the Special Function Registers. Above the Special Function Registers are the General Purpose Registers, implemented as Static RAM.

2.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 64 x 8 in the PIC10(L)F320/322. Each register is accessed, either directly or indirectly, through the File Select Register (FSR) (see Section 2.4 “Indirect Addressing, INDF and FSR Registers”).

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Table 2-3). These registers are static RAM.

The special registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the “core” are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.
2.2.2.1 STATUS Register

The STATUS register, shown in Register 2-1, contains:

- the arithmetic status of the ALU
- the Reset status
- the bank select bits for data memory (SRAM)

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS register as '000u u1uu' (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPP and MOVWF instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits (see Section 23.0 “Instruction Set Summary”).

**Note 1:** Bits IRP and RP1 of the STATUS register are not used by the PIC10(L)F320 and should be maintained as clear. Use of these bits is not recommended, since this may affect upward compatibility with future products.

**2:** The C and DC bits operate as a Borrow and Digit Borrow out bit, respectively, in subtraction.
**REGISTER 2-1: STATUS: STATUS REGISTER**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value at POR or BOR/Value at all other Resets</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>IRP: Reserved(2)</td>
<td></td>
</tr>
<tr>
<td>6-5</td>
<td>RP&lt;1:0&gt;: Reserved(2)</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>TO: Time-out bit</td>
<td>1 = After power-up, CLRWDT instruction or SLEEP instruction 0 = A WDT time-out occurred</td>
</tr>
<tr>
<td>3</td>
<td>PD: Power-Down bit</td>
<td>1 = After power-up or by the CLRWDT instruction 0 = By execution of the SLEEP instruction</td>
</tr>
<tr>
<td>2</td>
<td>Z: Zero bit</td>
<td>1 = The result of an arithmetic or logic operation is zero 0 = The result of an arithmetic or logic operation is not zero</td>
</tr>
<tr>
<td>1</td>
<td>DC: Digit Carry/Borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)(1)</td>
<td>1 = A carry-out from the 4th low-order bit of the result occurred 0 = No carry-out from the 4th low-order bit of the result</td>
</tr>
<tr>
<td>0</td>
<td>C: Carry/Borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)(1)</td>
<td>1 = A carry-out from the Most Significant bit of the result occurred 0 = No carry-out from the Most Significant bit of the result occurred</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **‘1’ = Bit is set**  
- **‘0’ = Bit is cleared**
- **q = Value depends on condition**  
- **-n/n = Value at POR and BOR at all other Resets**

**Note 1:** For **Borrow**, the polarity is reversed. A subtraction is executed by adding the two’s complement of the second operand. For rotate (**RRF, RLF**) instructions, this bit is loaded with either the high or low-order bit of the source register.

**2:** Maintain as ‘0’.
2.2.3 DEVICE MEMORY MAPS
The memory maps for PIC10(L)F320/322 are as shown in Table 2-2.

**TABLE 2-2: PIC10(L)F320/322 MEMORY MAP (BANK 0)**

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td>INDF(*)</td>
<td>Unimplemented data memory locations, read as '0'.</td>
</tr>
<tr>
<td>01h</td>
<td>TMR0</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>02h</td>
<td>PCL</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>03h</td>
<td>STATUS</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>04h</td>
<td>FSR</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>05h</td>
<td>PORTA</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>06h</td>
<td>TRISA</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>07h</td>
<td>LAT A</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>08h</td>
<td>ANSELA</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>09h</td>
<td>WPUA</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>0Ah</td>
<td>PCLATH</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>0Bh</td>
<td>INTCN</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>0Ch</td>
<td>PIR1</td>
<td>General Purpose Registers</td>
</tr>
<tr>
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<td>PIE1</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>0Eh</td>
<td>OPTION_REG</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>0Fh</td>
<td>PCON</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>10h</td>
<td>OSCCON</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>11h</td>
<td>TMR2</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>12h</td>
<td>PR2</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>13h</td>
<td>T2CON</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>14h</td>
<td>PWM1DCL</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>15h</td>
<td>PWM1DCH</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>16h</td>
<td>PWM1CON</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>17h</td>
<td>PWM2DCL</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>18h</td>
<td>PWM2DCH</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>19h</td>
<td>PWM2CON</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>1Ah</td>
<td>IOCAP</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>1Bh</td>
<td>IOCAN</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>1Ch</td>
<td>IOCAF</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>1Dh</td>
<td>FVRCON</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>1Eh</td>
<td>ADRES</td>
<td>General Purpose Registers</td>
</tr>
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<td>1Fh</td>
<td>ADCON</td>
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</tr>
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</tr>
<tr>
<td>21h</td>
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<td>General Purpose Registers</td>
</tr>
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<td>23h</td>
<td>PMDATH</td>
<td>General Purpose Registers</td>
</tr>
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</tr>
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<td>PMCON2</td>
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</tr>
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<td>26h</td>
<td>CLKRCON</td>
<td>General Purpose Registers</td>
</tr>
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<td>27h</td>
<td>NCO1ACCL</td>
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</tr>
<tr>
<td>29h</td>
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</tr>
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<td>2Ah</td>
<td>NCO1INCL</td>
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</tr>
<tr>
<td>2Bh</td>
<td>NCO1INCH</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>2Ch</td>
<td>Reserved</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>2Dh</td>
<td>NCO1CON</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>2Eh</td>
<td>NCO1CLK</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>2Fh</td>
<td>Reserved</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>30h</td>
<td>WDTCON</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>31h</td>
<td>CLC1CON</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>32h</td>
<td>CLC1SEL1</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>33h</td>
<td>CLC1SEL2</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>34h</td>
<td>CLC1POL</td>
<td>General Purpose Registers</td>
</tr>
<tr>
<td>35h</td>
<td>CLC1GLS0</td>
<td>General Purpose Registers</td>
</tr>
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<td>36h</td>
<td>CLC1GLS1</td>
<td>General Purpose Registers</td>
</tr>
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<td>CLC1GLS2</td>
<td>General Purpose Registers</td>
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<td>CLC1GLS3</td>
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</tr>
<tr>
<td>3Fh</td>
<td>BORCON</td>
<td>General Purpose Registers</td>
</tr>
</tbody>
</table>

Legend:
- ■ = Unimplemented data memory locations, read as ‘0’.
- * = Not a physical register.
### TABLE 2-3: SPECIAL FUNCTION REGISTER SUMMARY (BANK 0)

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOR</th>
<th>Value on all other resets</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td>INDF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>xxxxx xxxxx xxxxx xxxxx</td>
<td></td>
</tr>
<tr>
<td>01h</td>
<td>TMR0</td>
<td>Timer0 Module Register</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>xxxxx xxxxx xxxxx xxxxx</td>
<td></td>
</tr>
<tr>
<td>02h</td>
<td>PCL</td>
<td>Program Counter (PC) Least Significant Byte</td>
<td>0000 0000 0000 0000</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>03h</td>
<td>STATUS</td>
<td>IRP</td>
<td>RP1</td>
<td>RP0</td>
<td>TO</td>
<td>PD</td>
<td>Z</td>
<td>DC</td>
<td>C</td>
<td>0001 1xxx 000q guuuu</td>
<td></td>
</tr>
<tr>
<td>04h</td>
<td>FSR</td>
<td>Indirect Data Memory Address Pointer</td>
<td>xxxxx xxxxx xxxxx xxxxx</td>
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<td></td>
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<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>05h</td>
<td>PORTA</td>
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<td></td>
<td>RA3</td>
<td>RA2</td>
<td>RA1</td>
<td>RA0</td>
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<td>---- xxxx ---- ---- ----</td>
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<td>TRISA1</td>
<td>TRISA0</td>
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<td>---- 1111 ---- 1111</td>
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<td>LATA1</td>
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<td>ANSA1</td>
<td>ANSA0</td>
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</tr>
<tr>
<td>09h</td>
<td>WPUA</td>
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<td>WPUA2</td>
<td>WPUA1</td>
<td>WPUA0</td>
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<td>PCLH0</td>
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</tr>
<tr>
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<td>GIE</td>
<td>PEIE</td>
<td>TRM0IE</td>
<td>INTE</td>
<td>IOCIE</td>
<td>TRM0IF</td>
<td>INTF</td>
<td>IOCIF</td>
<td>0000 0000 0000 0000</td>
<td></td>
</tr>
<tr>
<td>0Ch</td>
<td>PIR1</td>
<td>ADIF</td>
<td></td>
<td>NCO1IF</td>
<td>CLC1IF</td>
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<td>TMR2IF</td>
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<td>CLC1IE</td>
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<td>WPUEN</td>
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<td>TOCS</td>
<td>TOSE</td>
<td>PSA</td>
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<td>BOR</td>
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</tr>
<tr>
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<td>Timer2 Module Register</td>
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</tr>
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<td>T2CKPS&lt;1:0&gt;</td>
<td></td>
<td>-000 0000 -000 0000</td>
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<td>PWM1DCL</td>
<td>PWM1DCL&lt;1:0&gt;</td>
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<td></td>
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<td></td>
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<td>xxxxx ---- ---- ---- ----</td>
<td></td>
</tr>
<tr>
<td>15h</td>
<td>PWM1DCH</td>
<td>PWM1DCH&lt;7:0&gt;</td>
<td>xxxxx xxxxx xxxxx xxxxx</td>
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</tr>
<tr>
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<td>PWM1EN</td>
<td>PWM1OE</td>
<td>PWM1OUT</td>
<td>PWM1POL</td>
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<td>PWM2DCL&lt;1:0&gt;</td>
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<td>PWM2OE</td>
<td>PWM2OUT</td>
<td>PWM2POL</td>
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<td>TSRNG</td>
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<td>ADFVR&lt;1:0&gt;</td>
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<td></td>
<td></td>
<td>ADON</td>
<td>xxxx xxxx xxxx xxxx</td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **x** = unknown,
- **u** = unchanged,
- **q** = value depends on condition,
- **-** = unimplemented, read as `'0'`.
- **r** = reserved.

**Note 1:** Unimplemented, read as `'1'`.© 2011-2015 Microchip Technology Inc.
**TABLE 2-3: SPECIAL FUNCTION REGISTER SUMMARY (BANK 0) (CONTINUED)**

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
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<td></td>
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<td>uuuu uuuu</td>
</tr>
</tbody>
</table>

**Legend:**
- x = unknown,
- u = unchanged,
- q = value depends on condition,
- - = unimplemented, read as ‘0’,
- r = reserved.

**Shaded locations are unimplemented, read as ‘0’.

**Note 1:** Unimplemented, read as ‘1’.

---

**TABLE 2-3 (Continued):**

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<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
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<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOR</th>
<th>Value on all other resets</th>
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<td>FREE</td>
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<tr>
<td>29h</td>
<td>NCO1ACCU</td>
<td>NCO1 Increment &lt;19..16&gt;</td>
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<td>NCO1 Increment &lt;15..8&gt;</td>
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</tbody>
</table>

**Legend:**
- x = unknown,
- u = unchanged,
- q = value depends on condition,
- - = unimplemented, read as ‘0’,
- r = reserved.

**Shaded locations are unimplemented, read as ‘0’.

**Note 1:** Unimplemented, read as ‘1’.
2.3 PCL and PCLATH

The Program Counter (PC) is 13 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any Reset, the PC is cleared. Figure 2-3 shows the two situations for the loading of the PC. The upper example in Figure 2-3 shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example in Figure 2-3 shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> → PCH).

**FIGURE 2-3: LOADING OF PC IN DIFFERENT SITUATIONS**

![Diagram showing PC loading](image)

2.3.1 MODIFYING PCL

Executing any instruction with the PCL register as the destination simultaneously causes the Program Counter PC<12:8> bits (PCH) to be replaced by the contents of the PCLATH register. This allows the entire contents of the program counter to be changed by writing the desired upper five bits to the PCLATH register. When the lower eight bits are written to the PCL register, all 13 bits of the program counter will change to the values contained in the PCLATH register and those being written to the PCL register.

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). Care should be exercised when jumping into a look-up table or program branch table (computed GOTO) by modifying the PCL register. Assuming that PCLATH is set to the table start address, if the table length is greater than 255 instructions or if the lower eight bits of the memory address rolls over from 0xFF to 0x00 in the middle of the table, then PCLATH must be incremented for each address rollover that occurs between the table beginning and the target location within the table.

For more information refer to Application Note AN556, “Implementation of a Table Read” (DS00556).

2.3.2 STACK

All devices have an 8-level x 13-bit wide hardware stack (see Figure 2-1). The stack space is not part of either program or data space and the Stack Pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

**Note 1:** There are no Status bits to indicate Stack Overflow or Stack Underflow conditions.

**Note 2:** There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions or the vectoring to an interrupt address.

2.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select Register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR and the IRP bit of the STATUS register, as shown in Figure 2-4.

A simple program to clear RAM location 40h-7Fh using indirect addressing is shown in Example 2-1.

**EXAMPLE 2-1: INDIRECT ADDRESSING**

```
MOVLW 0x40 ;initialize pointer
MOVWF FSR ;to RAM
NEXT CLRF INDF ;clear INDF register
INC FSR ;inc pointer
BTFSS FSR,7 ;all done?
GOTO NEXT ;no clear next
CONTINUE ;yes continue
```

FIGURE 2-4: DIRECT/INDIRECT ADDRESSING PIC10(L)F320/322

For memory map detail, see Figure 2-2.
3.0 DEVICE CONFIGURATION

Device configuration consists of Configuration Word and Device ID.

3.1 Configuration Word

There are several Configuration Word bits that allow different oscillator and memory protection options. These are implemented as Configuration Word at 2007h.
3.2 Register Definitions: Configuration Word

**REGISTER 3-1: CONFIG: CONFIGURATION WORD**

<table>
<thead>
<tr>
<th>bit 13</th>
<th>bit 8</th>
</tr>
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<tbody>
<tr>
<td>R/P-1/1</td>
<td>R/P-1/1</td>
</tr>
<tr>
<td>U-1</td>
<td>WRT&lt;1:0&gt;</td>
</tr>
</tbody>
</table>

**Legend:**

- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- '1' = Bit is set
- '0' = Bit is cleared
- P = Programmable bit

**Legend: 3:**

- 1 = Write protection off
- 0 = Write protection on

**Legend: 4:**

- 1 = Brown-out Reset voltage (VBOR), low trip point selected.
- 0 = Brown-out Reset voltage (VBOR), high trip point selected.

**Legend: 5:**

- 1 = Low-power Brown-out Reset Enable bit
- 0 = Low-power Brown-out Reset is disabled

**Legend: 6:**

- 1 = Low-Voltage Programming Enable bit
- 0 = High Voltage on MCLR/VPP must be used for programming

**Legend: 7:**

- 1 = Program memory code protection is disabled
- 0 = Program memory code protection is enabled

**Legend: 8:**

- 1 = MCLR/VPP pin function is MCLR; Weak pull-up enabled.
- 0 = MCLR/VPP pin function is digital input; MCLR internally disabled; Weak pull-up under control of WPUA3 bit.

**Note 1:**

- Enabling Brown-out Reset does not automatically enable Power-up Timer.

**Note 2:**

- Once enabled, code-protect can only be disabled by bulk erasing the device.

**Note 3:**

- See VBOR parameter for specific trip point voltages.
REGISTER 3-1:  CONFIG: CONFIGURATION WORD (CONTINUED)

bit 5  **PWRTE**: Power-up Timer Enable bit\(^{(1)}\)
      1 = PWRT disabled
      0 = PWRT enabled

bit 4-3  **WDTE\(<1:0>:** Watchdog Timer Enable bit
      11 = WDT enabled
      10 = WDT enabled while running and disabled in Sleep
      01 = WDT controlled by the SWDTEN bit in the WDTCON register
      00 = WDT disabled

bit 2-1  **BOREN\(<1:0>:** Brown-out Reset Enable bits
      11 = Brown-out Reset enabled; SBOREN bit is ignored
      10 = Brown-out Reset enabled while running, disabled in Sleep; SBOREN bit is ignored
      01 = Brown-out Reset controlled by the SBOREN bit in the BORCON register
      00 = Brown-out Reset disabled; SBOREN bit is ignored

bit 0  **FOSC**: Oscillator Selection bit
      1 = EC on CLKIN pin
      0 = INTOSC oscillator I/O function available on CLKIN pin

**Note** 1:  Enabling Brown-out Reset does not automatically enable Power-up Timer.
2:  Once enabled, code-protect can only be disabled by bulk erasing the device.
3:  See \textit{V\textsubscript{BOR}} parameter for specific trip point voltages.
3.3 Code Protection

Code protection allows the device to be protected from unauthorized access. Program memory protection and data memory protection are controlled independently. Internal access to the program memory and data memory are unaffected by any code protection setting.

3.3.1 PROGRAM MEMORY PROTECTION

The entire program memory space is protected from external reads and writes by the CP bit in Configuration Word. When CP = 0, external reads and writes of program memory are inhibited and a read will return all ‘0’s. The CPU can continue to read program memory, regardless of the protection bit settings. Writing the program memory is dependent upon the write protection setting. See Section 3.4 “Write Protection” for more information.

3.4 Write Protection

Write protection allows the device to be protected from unintended self-writes. Applications, such as boot loader software, can be protected while allowing other regions of the program memory to be modified.

The WRT<1:0> bits in Configuration Word define the size of the program memory block that is protected.

3.5 User ID

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are readable and writable during normal execution. See Section 3.6 “Device ID and Revision ID” for more information on accessing these memory locations. For more information on checksum calculation, see the “PIC10(L)F320/322 Flash Memory Programming Specification” (DS41572).
3.6 Device ID and Revision ID

The memory location 2006h is where the Device ID and Revision ID are stored. The upper nine bits hold the Device ID. The lower five bits hold the Revision ID. See Section 9.4 “User ID, Device ID and Configuration Word Access” for more information on accessing these memory locations.

Development tools, such as device programmers and debuggers, may be used to read the Device ID and Revision ID.

3.7 Register Definitions: Device and Revision

REGISTER 3-2: DEVID: DEVICE ID REGISTER(1)

<table>
<thead>
<tr>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
</tr>
</thead>
</table>
| | | | | | | DEV<8:3>| bit 13
| | | | | | | bit 8

<table>
<thead>
<tr>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
</tr>
</thead>
</table>
| | | | | | | DEV<2:0>| REV<4:0>| bit 7
| | | | | | | bit 0

Legend:
R = Readable bit
'1' = Bit is set
'0' = Bit is cleared

bit 13-5 DEVID<8:0>: Device ID bits

<table>
<thead>
<tr>
<th>Device</th>
<th>DEVID&lt;13:0&gt; Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC10F320</td>
<td>10 1001 101 x xxxx</td>
</tr>
<tr>
<td>PIC10LF320</td>
<td>10 1001 111 x xxxx</td>
</tr>
<tr>
<td>PIC10F322</td>
<td>10 1001 100 x xxxx</td>
</tr>
<tr>
<td>PIC10LF322</td>
<td>10 1001 110 x xxxx</td>
</tr>
</tbody>
</table>

bit 4-0 REV<4:0>: Revision ID bits
These bits are used to identify the revision.

Note 1: This location cannot be written.
4.0 OSCILLATOR MODULE

4.1 Overview

The oscillator module has a variety of clock sources and selection features that allow it to be used in a range of applications while maximizing performance and minimizing power consumption. Figure 4-1 illustrates a block diagram of the oscillator module.

The system can be configured to use an internal calibrated high-frequency oscillator as clock source, with a choice of selectable speeds via software.

Clock source modes are configured by the FOSC bit in Configuration Word (CONFIG).

1. EC oscillator from CLKIN.
2. INTOSC oscillator, CLKIN not enabled.

**FIGURE 4-1: PIC10(L)F320/322 CLOCK SOURCE BLOCK DIAGRAM**

**Note 1:** HFIOFR, HFIOFS and LFIOFR are Status bits in the OSCCON register.
4.2 Clock Source Modes

Clock source modes can be classified as external or internal.

- Internal clock source (INTOSC) is contained within the oscillator module, which has eight selectable output frequencies, with a maximum internal frequency of 16 MHz.
- The External Clock mode (EC) relies on an external signal for the clock source.

The system clock can be selected between external or internal clock sources via the FOSC bit of the Configuration Word.

4.3 Internal Clock Modes

The internal clock sources are contained within the oscillator module. The internal oscillator block has two internal oscillators that are used to generate all internal system clock sources: the 16 MHz High-Frequency Internal Oscillator (HFINTOSC) and the 31 kHz (LFINTOSC).

The HFINTOSC consists of a primary and secondary clock. The secondary clock starts first with rapid start-up time, but low accuracy. The secondary clock ready signal is indicated with the HFIOFR bit of the OSCCON register. The primary clock follows with slower start-up time and higher accuracy. The primary clock is stable when the HFIIOFS bit of the OSCCON register bit goes high.

4.3.1 INTOSC MODE

When the FOSC bit of the Configuration Word is cleared, the INTOSC mode is selected. When INTOSC is selected, CLKIN pin is available for general purpose I/O. See Section 3.0 “Device Configuration” for more information.

4.3.2 FREQUENCY SELECT BITS (IRCF)

The output of the 16 MHz HFINTOSC is connected to a divider and multiplexer (see Figure 4-1). The Internal Oscillator Frequency Select bits (IRCF) of the OSCCON register select the frequency output of the internal oscillator:

- HFINTOSC
  - 16 MHz
  - 8 MHz (default after Reset)
  - 4 MHz
  - 2 MHz
  - 1 MHz
  - 500 kHz
  - 250 kHz
- LFINTOSC
  - 31 kHz

Note: Following any Reset, the IRCF<2:0> bits of the OSCCON register are set to '110' and the frequency selection is set to 8 MHz. The user can modify the IRCF bits to select a different frequency.

There is no delay when switching between HFINTOSC frequencies with the IRCF bits. This is because the switch involves only a change to the frequency output divider.

Start-up delay specifications are located in Section 24.0 “Electrical Specifications”.
4.4 Register Definitions: Reference Clock Control

REGISTER 4-1: CLKRCON – REFERENCE CLOCK CONTROL REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>R/W-0/0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td>CLKROE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
-n = Value at POR  ‘1’ = Bit is set  ‘0’ = Bit is cleared  x = Bit is unknown
q = Value depends on condition

bit 7 Unimplemented: Read as ‘0’

bit 6
CLKROE: Reference Clock Output Enable bit
1 = Reference Clock output (CLKR), regardless of TRIS
0 = Reference Clock output disabled

bit 5-0 Unimplemented: Read as ‘0’

4.5 Register Definitions: Oscillator Control

REGISTER 4-2: OSCCON: OSCILLATOR CONTROL REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-0/0</th>
<th>R-0/0</th>
<th>U-0</th>
<th>R-0/0</th>
<th>R-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td>IRCF&lt;2:0&gt;</td>
<td>HFIOR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
u = Bit is unchanged  x = Bit is unknown  -n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set  ‘0’ = Bit is cleared  q = Value depends on condition

bit 7 Unimplemented: Read as ‘0’

bit 6-4
IRCF<2:0>: INTOSC (Fosc) Frequency Select bits
111 = 16 MHz
110 = 8 MHz (default value)
101 = 4 MHz
100 = 2 MHz
011 = 1 MHz
010 = 500 kHz
001 = 250 kHz
000 = 31 kHz (LFINTOSC)

bit 3 HFIOR: High-Frequency Internal Oscillator Ready bit
1 = 16 MHz Internal Oscillator (HFINTOSC) is ready
0 = 16 MHz Internal Oscillator (HFINTOSC) is not ready

bit 2 Unimplemented: Read as ‘0’

bit 1 LFIOR: Low-Frequency Internal Oscillator Ready bit
1 = 31 kHz Internal Oscillator (LFINTOSC) is ready
0 = 31 kHz Internal Oscillator (LFINTOSC) is not ready

bit 0 HFIOS: High-Frequency Internal Oscillator Stable bit
1 = 16 MHz Internal Oscillator (HFINTOSC) is stable
0 = 16 MHz Internal Oscillator (HFINTOSC) is not stable
4.6 External Clock Mode

4.6.1 EC MODE

The External Clock (EC) mode allows an externally generated logic level as the system clock source. When operating in this mode, an external clock source is connected to the CLKIN input.

### TABLE 4-1: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLKRCON</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>26</td>
</tr>
<tr>
<td>OSCCON</td>
<td>—</td>
<td>—</td>
<td>IRCF&lt;2:0&gt;</td>
<td>—</td>
<td>HFIOFR</td>
<td>—</td>
<td>LFIOFR</td>
<td>HFIOFS</td>
<td>26</td>
</tr>
</tbody>
</table>

**Legend:**
- × = unknown,
- ᵃ = unchanged,
- – = unimplemented locations read as '0'. Shaded cells are not used by ECWG.

### TABLE 4-2: SUMMARY OF CONFIGURATION WORD WITH CLOCK SOURCES

<table>
<thead>
<tr>
<th>Name</th>
<th>Bits</th>
<th>Bit 13/5</th>
<th>Bit 12/4</th>
<th>Bit 11/3</th>
<th>Bit 10/2</th>
<th>Bit 9/1</th>
<th>Bit 8/0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>CONFIG</td>
<td>13:8</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>WRT&lt;1:0&gt;</td>
<td>BORV</td>
<td>LPBOR</td>
<td>LVP</td>
</tr>
<tr>
<td></td>
<td>7:0</td>
<td>CP</td>
<td>MCLRE</td>
<td>PWRT</td>
<td>WDTE&lt;1:0&gt;</td>
<td>BOREN&lt;1:0&gt;</td>
<td>FOSC</td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.
5.0 RESETS

There are multiple ways to reset this device:

• Power-On Reset (POR)
• Brown-Out Reset (BOR)
• Low-Power Brown-Out Reset (LPBOR)
• MCLR Reset
• WDT Reset
• Programming mode exit

To allow VDD to stabilize, an optional Power-up Timer can be enabled to extend the Reset time after a BOR or POR event.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 5-1.

FIGURE 5-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

Note 1: See Table 5-1 for BOR active conditions.
5.1 Power-On Reset (POR)
The POR circuit holds the device in Reset until VDD has reached an acceptable level for minimum operation. Slow rising VDD, fast operating speeds or analog performance may require greater than minimum VDD. The PWRT, BOR or MCLR features can be used to extend the start-up period until all device operation conditions have been met.

5.1.1 POWER-UP TIMER (PWRT)
The Power-up Timer provides a nominal 64 ms time-out on POR or Brown-out Reset.
The device is held in Reset as long as PWRT is active. The PWRT delay allows additional time for the VDD to rise to an acceptable level. The Power-up Timer is enabled by clearing the PWRT<1:0> bit in Configuration Word.
The Power-up Timer starts after the release of the POR and BOR.
For additional information, refer to Application Note AN607, “Power-up Trouble Shooting” (DS00607).

5.2 Brown-Out Reset (BOR)
The BOR circuit holds the device in Reset when VDD reaches a selectable minimum level. Between the POR and BOR, complete voltage range coverage for execution protection can be implemented.
The Brown-out Reset module has four operating modes controlled by the BOREN<1:0> bits in Configuration Word. The four operating modes are:
- BOR is always on
- BOR is off when in Sleep
- BOR is controlled by software
- BOR is always off
Refer to Table 5-1 for more information.
The Brown-out Reset voltage level is selectable by configuring the BORV bit in Register 3-1.
A VDD noise rejection filter prevents the BOR from triggering on small events. If VDD falls below Vbor for a duration greater than parameter Tbordc, the device will reset. See Figure 5-2 for more information.

### TABLE 5-1: BOR OPERATING MODES

<table>
<thead>
<tr>
<th>BOREN&lt;1:0&gt;</th>
<th>SBOREN</th>
<th>Device Mode</th>
<th>BOR Mode</th>
<th>Device Operation upon: Release of POR/Wake-up from Sleep</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>X</td>
<td>X</td>
<td>Active</td>
<td>Waits for BOR ready&lt;1&gt; (BORRDY = 1)</td>
</tr>
<tr>
<td>10</td>
<td>X</td>
<td>Awake</td>
<td>Active</td>
<td>Waits for BOR ready (BORRDY = 1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sleep</td>
<td>Disabled</td>
<td></td>
</tr>
<tr>
<td>01</td>
<td>1</td>
<td>X</td>
<td>Active</td>
<td>Waits for BOR ready&lt;1&gt; (BORRDY = 1)</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>X</td>
<td>Disabled</td>
<td>Begins immediately (BORRDY = x)</td>
</tr>
<tr>
<td>00</td>
<td>X</td>
<td>X</td>
<td>Disabled</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: In these specific cases, “Release of POR” and “Wake-up from Sleep”, there is no delay in start-up. The BOR ready flag, (BORRDY = 1), will be set before the CPU is ready to execute instructions because the BOR circuit is forced on by the BOREN<1:0> bits.

5.2.1 BOR IS ALWAYS ON
When the BOREN bits of Configuration Word are programmed to ‘11’, the BOR is always on. The device start-up will be delayed until the BOR is ready and VDD is higher than the BOR threshold.
BOR protection is active during Sleep. The BOR does not delay wake-up from Sleep.

5.2.2 BOR IS OFF IN SLEEP
When the BOREN bits of Configuration Word are programmed to ‘10’, the BOR is on, except in Sleep. The device start-up will be delayed until the BOR is ready and VDD is higher than the BOR threshold.
BOR protection is not active during Sleep. The device wake-up will be delayed until the BOR is ready.

5.2.3 BOR CONTROLLED BY SOFTWARE
When the BOREN bits of Configuration Word are programmed to ‘01’, the BOR is controlled by the SBOREN bit of the BORCON register. The device start-up is not delayed by the BOR ready condition or the VDD level.
BOR protection begins as soon as the BOR circuit is ready. The status of the BOR circuit is reflected in the BORRDY bit of the BORCON register.
BOR protection is unchanged by Sleep.
### FIGURE 5-2: BROWN-OUT SITUATIONS

#### 5.3 Register Definition: BOR Control

**REGISTER 5-1: BORCON: BROWN-OUT RESET CONTROL REGISTER**

<table>
<thead>
<tr>
<th>R/W-1/u</th>
<th>R/W-0/u</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R-q/u</th>
</tr>
</thead>
<tbody>
<tr>
<td>SBOREN</td>
<td>BORFS(1)</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>BORRDY</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- {-n/n} = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **q** = Value depends on condition

**bit 7** **SBOREN**: Software Brown-out Reset Enable bit
- If BOREN <1:0> in Configuration Word = 01:
  - SBOREN is read/write, but has no effect on the BOR.
- If BOREN <1:0> in Configuration Word = 01:
  - 1 = BOR enabled
  - 0 = BOR disabled

**bit 6** **BORFS**: Brown-out Reset Fast Start bit(1)
- If BOREN<1:0> = 11 (Always on) or BOREN<1:0> = 00 (Always off)
  - BORFS is Read/Write, but has no effect.
- If BOREN<1:0> = 10 (Disabled in Sleep) or BOREN<1:0> = 01 (Under software control):
  - 1 = Band gap is forced on always (covers Sleep/wake-up/operating cases)
  - 0 = Band gap operates normally, and may turn off

**bit 5-1** **Unimplemented**: Read as ‘0’

**bit 0** **BORRDY**: Brown-out Reset Circuit Ready Status bit
- 1 = The Brown-out Reset circuit is active
- 0 = The Brown-out Reset circuit is inactive

**Note 1:** BOREN<1:0> bits are located in Configuration Word.
5.4 Low-Power Brown-out Reset (LPBOR)

The Low-Power Brown-Out Reset (LPBOR) is an essential part of the Reset subsystem. Refer to Figure 5-1 to see how the BOR interacts with other modules.

The LPBOR is used to monitor the external VDD pin. When too low of a voltage is detected, the device is held in Reset. When this occurs, a register bit (BOR) is changed to indicate that a BOR Reset has occurred. The same bit is set for both the BOR and the LPBOR. Refer to Register 5-2.

5.4.1 ENABLING LPBOR

The LPBOR is controlled by the LPBOR bit of Configuration Word. When the device is erased, the LPBOR module defaults to enabled.

5.5 MCLR

The MCLR is an optional external input that can reset the device. The MCLR function is controlled by the MCLRE and the LVP bit of Configuration Word (Table 5-2).

<table>
<thead>
<tr>
<th>TABLE 5-2: MCLR CONFIGURATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCLRE</td>
</tr>
<tr>
<td>-------</td>
</tr>
<tr>
<td>0</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>x</td>
</tr>
</tbody>
</table>

5.5.1 MCLR ENABLED

When MCLR is enabled and the pin is held low, the device is held in Reset. The MCLR pin is connected to VDD through an internal weak pull-up.

The device has a noise filter in the MCLR Reset path. The filter will detect and ignore small pulses.

Note: A Reset does not drive the MCLR pin low.

5.5.2 MCLR DISABLED

When MCLR is disabled, the pin functions as a general purpose input and the internal weak pull-up is under software control.

5.6 Watchdog Timer (WDT) Reset

The Watchdog Timer generates a Reset if the firmware does not issue a CLRWDT instruction within the time-out period. The TO and PD bits in the STATUS register are changed to indicate the WDT Reset. See Section 8.0 “Watchdog Timer” for more information.

5.7 Programming Mode ICSP Exit

Upon exit of Programming mode, the device will behave as if a POR had just occurred.

5.8 Power-Up Timer

The Power-up Timer optionally delays device execution after a BOR or POR event. This timer is typically used to allow VDD to stabilize before allowing the device to start running.

The Power-up Timer is controlled by the PWRTE bit of Configuration Word.

5.9 Start-up Sequence

Upon the release of a POR or BOR, the following must occur before the device will begin executing:
1. Power-up Timer runs to completion (if enabled).
2. MCLR must be released (if enabled).

The total time-out will vary based on oscillator configuration and Power-up Timer configuration. See Section 4.0 “Oscillator Module” for more information.

The Power-up Timer runs independently of MCLR Reset. If MCLR is kept low long enough, the Power-up Timer will expire. Upon bringing MCLR high, the device will begin execution after 10 Fosc cycles (see Figure 5-3). This is useful for testing purposes or to synchronize more than one device operating in parallel.
FIGURE 5-3:  RESET START-UP SEQUENCE

VDD
Internal POR
Power-Up Timer
MCLR
Internal RESET

Oscillator Modes

- Internal Oscillator
  Oscillator
  FOSC

- External Clock (EC)
  CLKIN
  FOSC
5.10 Determining the Cause of a Reset

Upon any Reset, multiple bits in the STATUS and PCON registers are updated to indicate the cause of the Reset. Table 5-3 and Table 5-4 show the Reset conditions of these registers.

### TABLE 5-3: RESET STATUS BITS AND THEIR SIGNIFICANCE

<table>
<thead>
<tr>
<th>POR</th>
<th>BOR</th>
<th>TO</th>
<th>PD</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>x</td>
<td>1</td>
<td>1</td>
<td>Power-on Reset</td>
</tr>
<tr>
<td>u</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Brown-out Reset</td>
</tr>
<tr>
<td>u</td>
<td>u</td>
<td>0</td>
<td>u</td>
<td>WDT Reset</td>
</tr>
<tr>
<td>u</td>
<td>u</td>
<td>0</td>
<td>0</td>
<td>WDT Wake-up from Sleep</td>
</tr>
<tr>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>MCLR Reset during normal operation</td>
</tr>
<tr>
<td>u</td>
<td>u</td>
<td>1</td>
<td>0</td>
<td>MCLR Reset during Sleep</td>
</tr>
</tbody>
</table>

### TABLE 5-4: RESET CONDITION FOR SPECIAL REGISTERS

<table>
<thead>
<tr>
<th>Condition</th>
<th>Program Counter</th>
<th>STATUS Register</th>
<th>PCON Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power-on Reset</td>
<td>0000h</td>
<td>0001 1000</td>
<td>----- --0x</td>
</tr>
<tr>
<td>MCLR Reset during normal operation</td>
<td>0000h</td>
<td>000u uuuu</td>
<td>----- --uu</td>
</tr>
<tr>
<td>MCLR Reset during Sleep</td>
<td>0000h</td>
<td>0001 0uuu</td>
<td>----- --uu</td>
</tr>
<tr>
<td>WDT Reset</td>
<td>0000h</td>
<td>0000 uuuu</td>
<td>----- --uu</td>
</tr>
<tr>
<td>WDT Wake-up from Sleep</td>
<td>PC + 1</td>
<td>0000 0uuu</td>
<td>----- --uu</td>
</tr>
<tr>
<td>Brown-out Reset</td>
<td>0000h</td>
<td>0001 1uuu</td>
<td>----- --u0</td>
</tr>
<tr>
<td>Interrupt Wake-up from Sleep</td>
<td>PC + 1 (1)</td>
<td>0001 0uuu</td>
<td>----- --uu</td>
</tr>
</tbody>
</table>

Legend:  u = unchanged,  x = unknown,  - = unimplemented bit, reads as '0'.

**Note 1:** When the wake-up is due to an interrupt and Global Enable bit (GIE) is set, the return address is pushed on the stack and PC is loaded with the interrupt vector (0004h) after execution of PC + 1.
5.11 Power Control (PCON) Register

The Power Control (PCON) register contains flag bits to differentiate between a:

* Power-On Reset (POR)
* Brown-Out Reset (BOR)

The PCON register bits are shown in Register 5-2.

5.12 Register Definition: Power Control

### REGISTER 5-2: PCON: POWER CONTROL REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W/HC-q/u</th>
<th>R/W/HC-q/u</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>POR</td>
<td>BOR</td>
</tr>
</tbody>
</table>

Legend:

- HC = Bit is cleared by hardware
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- q = Value depends on condition

bit 7-2 Unimplemented: Read as ‘0’

bit 1 **POR:** Power-on Reset Status bit

- 1 = No Power-on Reset occurred
- 0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **BOR:** Brown-out Reset Status bit

- 1 = No Brown-out Reset occurred
- 0 = A Brown-out Reset occurred (must be set in software after a Power-on Reset or Brown-out Reset occurs)

### TABLE 5-5: SUMMARY OF REGISTERS ASSOCIATED WITH RESETS

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>BORCON</td>
<td>SBOREN</td>
<td>BORFS</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>BORRDY 30</td>
</tr>
<tr>
<td>PCON</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>POR</td>
<td>BOR</td>
<td>34</td>
</tr>
<tr>
<td>STATUS</td>
<td>IRP</td>
<td>RP1</td>
<td>RP0</td>
<td>TO</td>
<td>PD</td>
<td>Z</td>
<td>DC</td>
<td>C</td>
<td>13</td>
</tr>
<tr>
<td>WDTCON</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>WDTPS&lt;4:0&gt;</td>
<td>SWDTE&lt;4:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td>48</td>
</tr>
</tbody>
</table>

Legend: — = unimplemented location, read as ‘0’. Shaded cells are not used by Resets.

### TABLE 5-6: SUMMARY OF CONFIGURATION WORD WITH RESETS

<table>
<thead>
<tr>
<th>Name</th>
<th>Bits</th>
<th>Bit -/7</th>
<th>Bit -/6</th>
<th>Bit 13/5</th>
<th>Bit 12/4</th>
<th>Bit 11/3</th>
<th>Bit 10/2</th>
<th>Bit 9/1</th>
<th>Bit 8/0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>CONFIG</td>
<td>13:8</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>WRT&lt;1:0&gt;</td>
<td>BORV</td>
<td>LPBOR</td>
<td>LVP</td>
<td>—</td>
<td>20</td>
</tr>
<tr>
<td></td>
<td>7:0</td>
<td>CP</td>
<td>MCLRE</td>
<td>PWLTE</td>
<td>WDTE&lt;1:0&gt;</td>
<td>BOREN&lt;1:0&gt;</td>
<td>FOSC</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend: — = unimplemented location, read as ‘0’. Shaded cells are not used by Reset.
6.0 INTERRUPTS

The interrupt feature allows certain events to preempt normal program flow. Firmware is used to determine the source of the interrupt and act accordingly. Some interrupts can be configured to wake the MCU from Sleep mode.

This chapter contains the following information for Interrupts:
- Operation
- Interrupt Latency
- Interrupts During Sleep
- INT Pin
- Context Saving during Interrupts

Many peripherals produce interrupts. Refer to the corresponding chapters for details.

A block diagram of the interrupt logic is shown in Figure 6-1.

FIGURE 6-1: INTERRUPT LOGIC
6.1 Operation

Interrupts are disabled upon any device Reset. They are enabled by setting the following bits:

- GIE bit of the INTCON register
- Interrupt Enable bit(s) for the specific interrupt event(s)
- PEIE bit of the INTCON register (if the Interrupt Enable bit of the interrupt event is contained in the PIE1 register)

The INTCON and PIR1 registers record individual interrupts via interrupt flag bits. Interrupt flag bits will be set, regardless of the status of the GIE, PEIE and individual interrupt enable bits.

The following events happen when an interrupt event occurs while the GIE bit is set:

- Current prefetched instruction is flushed
- GIE bit is cleared
- Current Program Counter (PC) is pushed onto the stack
- PC is loaded with the interrupt vector 0004h

The firmware within the Interrupt Service Routine (ISR) should determine the source of the interrupt by polling the interrupt flag bits. The interrupt flag bits must be cleared before exiting the ISR to avoid repeated interrupts. Because the GIE bit is cleared, any interrupt that occurs while executing the ISR will be recorded through its interrupt flag, but will not cause the processor to redirect to the interrupt vector.

The `RETFIE` instruction exits the ISR by popping the previous address from the stack, and setting the GIE bit.

For additional information on a specific interrupt's operation, refer to its peripheral chapter.

6.2 Interrupt Latency

Interrupt latency is defined as the time from when the interrupt event occurs to the time code execution at the interrupt vector begins. The latency for synchronous interrupts is three or four instruction cycles. For asynchronous interrupts, the latency is three to five instruction cycles, depending on when the interrupt occurs. See Figure 6-2 and Section 6.3 “Interrupts During Sleep” for more details.

Note 1: Individual interrupt flag bits are set, regardless of the state of any other enable bits.

2: All interrupts will be ignored while the GIE bit is cleared. Any interrupt occurring while the GIE bit is clear will be serviced when the GIE bit is set again.
**FIGURE 6-2: INTERRUPT LATENCY**

The diagram illustrates the interrupt latency in the PIC10(L)F320/322 microcontrollers. It shows the sequence of events and timings for different types of instructions (1 cycle, 2 cycle, and 3 cycle) following an interrupt sampled during Q1.

- **INTOSC** (Interrupt Oscillator): The timing events related to interrupt sampling.
- **CLKR** (Clock Reset): Sequences related to clock reset.
- **GIE** (Global Enable): The enable status of interrupts.
- **PC** (Program Counter): Current and new program counter values.
- **FSR ADDR** (File Select Register Address): Addresses involved in FSR operations.
- **Executes** (Instructions at PC): Instructions executed at the program counter.

The diagram uses specific labels and timing notations to detail the interrupt handling process, including the execution of different instruction lengths and their impacts on the program counter and file select register addresses.
**FIGURE 6-3: INT PIN INTERRUPT TIMING**

<table>
<thead>
<tr>
<th>INTOSC</th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLKR</td>
<td>(3)</td>
<td></td>
<td></td>
<td></td>
<td>(1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INT pin</td>
<td></td>
<td>(1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INTF</td>
<td>(4)</td>
<td></td>
<td>Interrupt Latency [2]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GIE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**INSTRUCTION FLOW**

- **PC**: PC, PC + 1, PC + 1, 0004h, 0005h

- **Instruction Fetched**: Inst (PC), Inst (PC + 1), —, Inst (0004h), Inst (0005h)

- **Instruction Executed**: Inst (PC - 1), Inst (PC), Forced NOP, Forced NOP, Inst (0004h)

**Note**: 1. INTF flag is sampled here (every Q1).
2. Asynchronous interrupt latency = 3-5 Tcy. Synchronous latency = 3-4 Tcy, where Tcy = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.
3. For minimum width of INT pulse, refer to AC specifications in Section 24.0 “Electrical Specifications”.
4. INTF is enabled to be set any time during the Q4-Q1 cycles.
6.3 Interrupts During Sleep

Some interrupts can be used to wake from Sleep. To wake from Sleep, the peripheral must be able to operate without the system clock. The interrupt source must have the appropriate Interrupt Enable bit(s) set prior to entering Sleep.

On waking from Sleep, if the GIE bit is also set, the processor will branch to the interrupt vector. Otherwise, the processor will continue executing instructions after the SLEEP instruction. The instruction directly after the SLEEP instruction will always be executed before branching to the ISR. Refer to the Section 7.0 “Power-Down Mode (Sleep)” for more details.

6.4 INT Pin

The INT pin can be used to generate an asynchronous edge-triggered interrupt. This interrupt is enabled by setting the INTE bit of the INTCON register. The INTEDG bit of the OPTION_REG register determines on which edge the interrupt will occur. When the INTEDG bit is set, the rising edge will cause the interrupt. When the INTEDG bit is clear, the falling edge will cause the interrupt. The INTF bit of the INTCON register will be set when a valid edge appears on the INT pin. If the GIE and INTE bits are also set, the processor will redirect program execution to the interrupt vector.

6.5 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (e.g., W and STATUS registers). This must be implemented in software.

Temporary holding registers W_TEMP and STATUS_TEMP should be placed in the last 16 bytes of GPR (see Table 1-2). This makes context save and restore operations simpler. The code shown in Example 6-1 can be used to:

- Store the W register
- Store the STATUS register
- Execute the ISR code
- Restore the Status (and Bank Select Bit register)
- Restore the W register

Note: These devices do not require saving the PCLATH. However, if computed GOTOs are used in both the ISR and the main code, the PCLATH must be saved and restored in the ISR.

EXAMPLE 6-1: SAVING STATUS AND W REGISTERS IN RAM

```
  MOVWF W_TEMP ;Copy W to TEMP register
  SWAPF STATUS,W ;Swap status to be saved into W
                 ;Swaps are used because they do not affect the status bits
  MOVWF STATUS_TEMP ;Save status to bank zero STATUS_TEMP register
  ;(ISR)
  ;Insert user code here
  SWAPF STATUS_TEMP,W ;Swap STATUS_TEMP register into W
                       ;(sets bank to original state)
  MOVWF STATUS ;Move W into STATUS register
  SWAPF W_TEMP,F ;Swap W_TEMP
  SWAPF W_TEMP,W ;Swap W_TEMP into W
```

6.6 Interrupt Control Registers

REGISTER 6-1: INTCON: INTERRUPT CONTROL REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIE</td>
<td>PEIE</td>
<td>TMR0IE</td>
<td>INTE</td>
<td>IOCIE</td>
<td>TMR0IF</td>
<td>INTF</td>
<td>IOCIF(1)</td>
</tr>
</tbody>
</table>

Legend:

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
u = Bit is unchanged
x = Bit is unknown
-\(n/n\) = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set
‘0’ = Bit is cleared

bit 7 GIE: Global Interrupt Enable bit
  1 = Enables all active interrupts
  0 = Disables all interrupts

bit 6 PEIE: Peripheral Interrupt Enable bit
  1 = Enables all active peripheral interrupts
  0 = Disables all peripheral interrupts

bit 5 TMR0IE: Timer0 Overflow Interrupt Enable bit
  1 = Enables the Timer0 interrupt
  0 = Disables the Timer0 interrupt

bit 4 INTE: INT External Interrupt Enable bit
  1 = Enables the INT external interrupt
  0 = Disables the INT external interrupt

bit 3 IOCIE: Interrupt-on-Change Interrupt Enable bit
  1 = Enables the interrupt-on-change interrupt
  0 = Disables the interrupt-on-change interrupt

bit 2 TMR0IF: Timer0 Overflow Interrupt Flag bit
  1 = TMR0 register has overflowed
  0 = TMR0 register did not overflow

bit 1 INTF: INT External Interrupt Flag bit
  1 = The INT external interrupt occurred
  0 = The INT external interrupt did not occur

bit 0 IOCIF: Interrupt-on-Change Interrupt Flag bit(1)
  1 = When at least one of the interrupt-on-change pins changed state
  0 = None of the interrupt-on-change pins have changed state

Note 1: The IOCIF Flag bit is read-only and cleared when all the Interrupt-on-Change flags in the IOCAF register have been cleared by software.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Interrupt Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.
### REGISTER 6-2: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

<table>
<thead>
<tr>
<th>U-0</th>
<th>R/W-0/0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ADIE</td>
<td>NCO1IE</td>
<td>CLC1IE</td>
<td>TMR2IE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

**Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as ‘0’**

**Legend:**
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared

| bit 7 | **Unimplemented:** Read as ‘0’ |
| bit 6 | **ADIE:** A/D Converter Interrupt Enable bit |
|       | 1 = Enables the A/D converter interrupt |
|       | 0 = Disables the A/D converter interrupt |
| bit 5 | **Unimplemented:** Read as ‘0’ |
| bit 4 | **NCO1IE:** Numerically Controlled Oscillator Interrupt Enable bit |
|       | 1 = Enables the NCO overflow interrupt |
|       | 0 = Disables the NCO overflow interrupt |
| bit 3 | **CLC1IE:** Configurable Logic Block Interrupt Enable bit |
|       | 1 = Enables the CLC interrupt |
|       | 0 = Disables the CLC interrupt |
| bit 2 | **Unimplemented:** Read as ‘0’ |
| bit 1 | **TMR2IE:** TMR2 to PR2 Match Interrupt Enable bit |
|       | 1 = Enables the TMR2 to PR2 Match interrupt |
|       | 0 = Disables the TMR2 to PR2 Match interrupt |
| bit 0 | **Unimplemented:** Read as ‘0’ |

**Note:** Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.
REGISTER 6-3: PIR1: PERIPHERAL INTERRUPT REQUEST REGISTER 1

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>ADIF</td>
<td>NCO1IF</td>
</tr>
<tr>
<td>R/W-0/0</td>
<td>U-0</td>
</tr>
<tr>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>CLC1IF</td>
<td>TMR2IF</td>
</tr>
<tr>
<td>U-0</td>
<td>R/W-0/0</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared

- **bit 7**: Unimplemented: Read as '0'
- **bit 6**: ADIF: A/D Converter Interrupt Flag bit
  - 1 = The A/D conversion completed
  - 0 = The A/D conversion is not complete
- **bit 5**: Unimplemented: Read as '0'
- **bit 4**: NCO1IF: Numerically Controlled Oscillator Interrupt Flag bit
  - 1 = NCO1 overflow occurred (must be cleared in software)
  - 0 = No NCO1 overflow
- **bit 3**: CLC1IF: Configurable Logic Block Rising Edge Interrupt Flag bit
  - 1 = CLC interrupt occurred (must be cleared in software)
  - 0 = No CLC Interrupt
- **bit 2**: Unimplemented: Read as '0'
- **bit 1**: TMR2IF: TMR2 to PR2 Match Interrupt Flag bit
  - 1 = TMR2 to PR2 match occurred (must be cleared in software)
  - 0 = No TMR2 to PR2 match
  - **Note**: The match must occur the number of times specified by the TMR2 postscaler (Register 17-1).
- **bit 0**: Unimplemented: Read as '0'

**Note**: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Interrupt Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.
TABLE 6-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>TMR0IE</td>
<td>INTE</td>
<td>IOCIE</td>
<td>TMR0IF</td>
<td>INTF</td>
<td>IOCIF</td>
<td>40</td>
</tr>
<tr>
<td>IOCAF</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>76</td>
</tr>
<tr>
<td>IOCAN</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>75</td>
</tr>
<tr>
<td>IOCAP</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>75</td>
</tr>
<tr>
<td>OPTION_REG</td>
<td>WPUEN</td>
<td>INTEDG</td>
<td>T0CS</td>
<td>T0SE</td>
<td>PSA</td>
<td>—</td>
<td>—</td>
<td>PS&lt;2:0&gt;</td>
<td>95</td>
</tr>
<tr>
<td>PIE1</td>
<td>—</td>
<td>ADIE</td>
<td>—</td>
<td>NCO1IE</td>
<td>CLC1IE</td>
<td>—</td>
<td>—</td>
<td>TMR2IE</td>
<td>41</td>
</tr>
<tr>
<td>PIR1</td>
<td>—</td>
<td>ADIF</td>
<td>—</td>
<td>NCO1IF</td>
<td>CLC1IF</td>
<td>—</td>
<td>—</td>
<td>TMR2IF</td>
<td>42</td>
</tr>
</tbody>
</table>

Legend: — = unimplemented location, read as ‘0’. Shaded cells are not used by Interrupts.
7.0 POWER-DOWN MODE (SLEEP)

The Power-Down mode is entered by executing a SLEEP instruction.

Upon entering Sleep mode, the following conditions exist:

1. WDT will be cleared but keeps running, if enabled for operation during Sleep.
2. PD bit of the STATUS register is cleared.
3. TO bit of the STATUS register is set.
4. CPU clock is disabled.
5. 31 kHz LFINTOSC is unaffected and peripherals that operate from it may continue operation in Sleep.
6. ADC is unaffected, if the dedicated FRC clock is selected.
7. I/O ports maintain the status they had before SLEEP was executed (driving high, low or high-impedance).
8. Resets other than WDT are not affected by Sleep mode.

Refer to individual chapters for more details on peripheral operation during Sleep.

To minimize current consumption, the following conditions should be considered:

- I/O pins should not be floating
- External circuitry sinking current from I/O pins
- Internal circuitry sourcing current from I/O pins
- Current draw from pins with internal weak pull-ups
- Modules using 31 kHz LFINTOSC
- CWG and NCO modules using HFINTOSC

I/O pins that are high-impedance inputs should be pulled to VDD or VSS externally to avoid switching currents caused by floating inputs.

Examples of internal circuitry that might be sourcing current include the FVR module. See Section 12.0 “Fixed Voltage Reference (FVR)” for more information on these modules.

7.1 Wake-up from Sleep

The device can wake-up from Sleep through one of the following events:

1. External Reset input on MCLR pin, if enabled
2. BOR Reset, if enabled
3. POR Reset
4. Watchdog Timer, if enabled
5. Any external interrupt
6. Interrupts by peripherals capable of running during Sleep (see individual peripheral for more information)

The first three events will cause a device Reset. The last three events are considered a continuation of program execution. To determine whether a device Reset or wake-up event occurred, refer to Section 5.10 “Determining the Cause of a Reset”.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is prefetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be enabled. Wake-up will occur regardless of the state of the GIE bit. If the GIE bit is disabled, the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is enabled, the device executes the instruction after the SLEEP instruction, the device will then call the Interrupt Service Routine. In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

The WDT is cleared when the device wakes up from Sleep, regardless of the source of wake-up.

The Complementary Waveform Generator (CWG) and the Numerically Controlled Oscillator (NCO) modules can utilize the HFINTOSC oscillator as their respective clock source. Under certain conditions, when the HFINTOSC is selected for use with the CWG or NCO modules, the HFINTOSC will remain active during Sleep. This will have a direct effect on the Sleep mode current. Please refer to 21.0 “Complementary Waveform Generator (CWG) Module” and 20.0 “Numerically Controlled Oscillator (NCO) Module” for more information.
### 7.1.1 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a SLEEP instruction
  - SLEEP instruction will execute as a NOP.
  - WDT and WDT prescaler will not be cleared
  - TO bit of the STATUS register will not be set
  - PD bit of the STATUS register will not be cleared.

- If the interrupt occurs **during or after** the execution of a SLEEP instruction
  - SLEEP instruction will be completely executed
  - Device will immediately wake-up from Sleep
  - WDT and WDT prescaler will be cleared
  - TO bit of the STATUS register will be set
  - PD bit of the STATUS register will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the PD bit. If the PD bit is set, the SLEEP instruction was executed as a NOP.

**FIGURE 7-1: WAKE-UP FROM SLEEP THROUGH INTERRUPT**

**TABLE 7-1: SUMMARY OF REGISTERS ASSOCIATED WITH POWER-DOWN MODE**

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>STATUS</td>
<td>IRP</td>
<td>RP1</td>
<td>RP0</td>
<td>TO</td>
<td>PD</td>
<td>Z</td>
<td>DC</td>
<td>C</td>
<td>13</td>
</tr>
<tr>
<td>WDTCON</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>WDTPS&lt;4:0&gt;</td>
<td>—</td>
<td>SWDTEN</td>
<td>48</td>
<td></td>
</tr>
</tbody>
</table>

**Legend:** — = unimplemented location, read as ‘0’. Shaded cells are not used in Power-down mode.
8.0 WATCHDOG TIMER

The Watchdog Timer is a system timer that generates a Reset if the firmware does not issue a CLRWDT instruction within the time-out period. The Watchdog Timer is typically used to recover the system from unexpected events.

The WDT has the following features:

- Independent clock source
- Multiple operating modes
  - WDT is always on
  - WDT is off when in Sleep
  - WDT is controlled by software
  - WDT is always off
- Configurable time-out period is from 1 ms to 256 seconds (typical)
- Multiple Reset conditions
- Operation during Sleep

FIGURE 8-1: WATCHDOG TIMER BLOCK DIAGRAM

![Watchdog Timer Block Diagram](image_url)
8.1 Independent Clock Source
The WDT derives its time base from the 31 kHz LFINTOSC internal oscillator. Time intervals in this chapter are based on a nominal interval of 1ms. See Section 24.0 “Electrical Specifications” for the LFINTOSC tolerances.

8.2 WDT Operating Modes
The Watchdog Timer module has four operating modes controlled by the WDTE<1:0> bits in Configuration Word. See Table 8-1.

8.2.1 WDT IS ALWAYS ON
When the WDTE bits of Configuration Word are set to '11', the WDT is always on.
WDT protection is active during Sleep.

8.2.2 WDT IS OFF IN SLEEP
When the WDTE bits of Configuration Word are set to '10', the WDT is on, except in Sleep.
WDT protection is not active during Sleep.

8.2.3 WDT CONTROLLED BY SOFTWARE
When the WDTE bits of Configuration Word are set to '01', the WDT is controlled by the SWDTEN bit of the WDTCON register.
WDT protection is unchanged by Sleep. See Table 8-1 for more details.

8.3 Time-Out Period
The WDTPS bits of the WDTCON register set the time-out period from 1 ms to 256 seconds (nominal). After a Reset, the default time-out period is 2 seconds.

8.4 Clearing the WDT
The WDT is cleared when any of the following conditions occur:
- Any Reset
- CLRWDT instruction is executed
- Device enters Sleep
- Device wakes up from Sleep
- Oscillator fail
- WDT is disabled
See Table 8-2 for more information.

8.5 Operation During Sleep
When the device enters Sleep, the WDT is cleared. If the WDT is enabled during Sleep, the WDT resumes counting.

When the device exits Sleep, the WDT is cleared again.

When a WDT time-out occurs while the device is in Sleep, no Reset is generated. Instead, the device wakes up and resumes operation. The TO and PD bits in the STATUS register are changed to indicate the event. See Section 2.0 “Memory Organization” and Register 2-1 for more information.

<table>
<thead>
<tr>
<th>WDTE&lt;1:0&gt;</th>
<th>SWDTEN</th>
<th>Device Mode</th>
<th>WDT Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>X</td>
<td>X</td>
<td>Active</td>
</tr>
<tr>
<td>10</td>
<td>X</td>
<td>Awake</td>
<td>Active</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sleep</td>
<td>Disabled</td>
</tr>
<tr>
<td>01</td>
<td>1</td>
<td>X</td>
<td>Active</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td></td>
<td>Disabled</td>
</tr>
<tr>
<td>00</td>
<td>X</td>
<td>X</td>
<td>Disabled</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Conditions</th>
<th>WDT</th>
</tr>
</thead>
<tbody>
<tr>
<td>WDTE&lt;1:0&gt; = 00</td>
<td></td>
</tr>
<tr>
<td>WDTE&lt;1:0&gt; = 01 and SWDTEN = 0</td>
<td></td>
</tr>
<tr>
<td>WDTE&lt;1:0&gt; = 10 and enter Sleep</td>
<td></td>
</tr>
<tr>
<td>CLRWDT Command</td>
<td></td>
</tr>
<tr>
<td>Exit Sleep</td>
<td></td>
</tr>
<tr>
<td>Change INTOSC divider (IRCF bits)</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Conditions</th>
<th>WDT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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8.6 Watchdog Control Register

REGISTER 8-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

<table>
<thead>
<tr>
<th>bit 7-6</th>
<th>bit 5-1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unimplemented</td>
<td>WDTPS&lt;4:0&gt;: Watchdog Timer Period Select bits&lt;sup&gt;1&lt;/sup&gt;</td>
<td>SWDTEN</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- -n/n = Value at POR and BOR/Value at all other Resets

- **bit 7-6**
  - **Unimplemented**: Read as ‘0’

- **bit 5-1**
  - **WDTPS<4:0>:** Watchdog Timer Period Select bits<sup>1</sup>
    - **Bit Value = Prescale Rate**
      - **11111** = Reserved. Results in minimum interval (1:32)
      - ... (other prescale rates listed)
      - **10011** = 1:8388608 (2<sup>23</sup>) (Interval 256s nominal)
      - **10010** = 1:4194304 (2<sup>22</sup>) (Interval 128s nominal)
      - **10001** = 1:2097152 (2<sup>21</sup>) (Interval 64s nominal)
      - **10000** = 1:1048576 (2<sup>20</sup>) (Interval 32s nominal)
      - **01111** = 1:524288 (2<sup>19</sup>) (Interval 16s nominal)
      - **01110** = 1:262144 (2<sup>18</sup>) (Interval 8s nominal)
      - **01101** = 1:131072 (2<sup>17</sup>) (Interval 4s nominal)
      - **01100** = 1:65536 (Interval 2s nominal) (Reset value)
      - **0101</sup> = 1:32768 (Interval 1s nominal)
      - **01001** = 1:16384 (Interval 512 ms nominal)
      - **01000** = 1:8192 (Interval 256 ms nominal)
      - **00111** = 1:4096 (Interval 128 ms nominal)
      - **00110** = 1:2048 (Interval 64 ms nominal)
      - **00101** = 1:1024 (Interval 32 ms nominal)
      - **00100** = 1:512 (Interval 16 ms nominal)
      - **00011** = 1:256 (Interval 8 ms nominal)
      - **00010** = 1:128 (Interval 4 ms nominal)
      - **00001** = 1:64 (Interval 2 ms nominal)
      - **00000** = 1:32 (Interval 1 ms nominal)

- **bit 0**
  - **SWDTEN: Software Enable/Disable for Watchdog Timer bit**
    - **If WDTE<1:0> = 00:**
      - This bit is ignored.
    - **If WDTE<1:0> = 01:**
      - **1** = WDT is turned on
      - **0** = WDT is turned off
    - **If WDTE<1:0> = 1x:**
      - This bit is ignored.

**Note 1:** Times are approximate. WDT time is based on 31 kHz LFINTOSC.
### TABLE 8-3: SUMMARY OF REGISTERS ASSOCIATED WITH WATCHDOG TIMER

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>OSCCON</td>
<td>—</td>
<td>IRCF&lt;2:0&gt;</td>
<td>HFIOFR</td>
<td>—</td>
<td>LFIOFR</td>
<td>HFIOFS</td>
<td></td>
<td></td>
<td>26</td>
</tr>
<tr>
<td>STATUS</td>
<td>IRP</td>
<td>RP1</td>
<td>RP0</td>
<td>TO</td>
<td>P0</td>
<td>Z</td>
<td>DC</td>
<td>C</td>
<td>13</td>
</tr>
<tr>
<td>WDTCON</td>
<td>—</td>
<td>—</td>
<td>WDTPS&lt;4:0&gt;</td>
<td></td>
<td>SWDTEN</td>
<td></td>
<td></td>
<td></td>
<td>48</td>
</tr>
</tbody>
</table>

**Legend:**  
x = unknown, u = unchanged, – = unimplemented locations read as ‘0’. Shaded cells are not used by Watchdog Timer.

### TABLE 8-4: SUMMARY OF CONFIGURATION WORD WITH WATCHDOG TIMER

<table>
<thead>
<tr>
<th>Name</th>
<th>Bits</th>
<th>Bit 13/5</th>
<th>Bit 12/4</th>
<th>Bit 11/3</th>
<th>Bit 10/2</th>
<th>Bit 9/1</th>
<th>Bit 8/0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>CONFIG</td>
<td>13:8</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>WRT&lt;1:0&gt;</td>
<td>BORV</td>
<td>LPBOR</td>
<td>LVP</td>
</tr>
<tr>
<td></td>
<td>7:0</td>
<td>CP</td>
<td>MCLRE</td>
<td>PWRTE</td>
<td>WDTE&lt;1:0&gt;</td>
<td>BOREN&lt;1:0&gt;</td>
<td>FOSC</td>
<td>20</td>
</tr>
</tbody>
</table>

**Legend:** — = unimplemented location, read as ‘0’. Shaded cells are not used by Watchdog Timer.
9.0 FLASH PROGRAM MEMORY CONTROL

The Flash program memory is readable and writable during normal operation over the full VDD range. Program memory is indirectly addressed using Special Function Registers (SFRs). The SFRs used to access program memory are:

- PMCON1
- PMCON2
- PMDATL
- PMDATH
- PMADRL
- PMADRH

When accessing the program memory, the PMDATH:PMDATL register pair forms a 2-byte word that holds the 14-bit data for read/write, and the PMADRH:PMADRL register pair forms a 2-byte word that holds the 9-bit address of the program memory location being read.

The write time is controlled by an on-chip timer. The write/erase voltages are generated by an on-chip charge pump rated to operate over the operating voltage range of the device.

The Flash program memory can be protected in two ways; by code protection (CP bit in Configuration Word) and write protection (WRT<1:0> bits in Configuration Word).

Code protection (CP = 0) disables access, reading and writing, to the Flash program memory via external device programmers. Code protection does not affect the self-write and erase functionality. Code protection can only be reset by a device programmer performing a Bulk Erase to the device, clearing all Flash program memory, Configuration bits and User IDs.

Write protection prohibits self-write and erase to a portion or all of the Flash program memory as defined by the bits WRT<1:0>. Write protection does not affect a device programmers ability to read, write or erase the device.

9.1 PMADRL and PMADRH Registers

The PMADRH:PMADRL register pair can address up to a maximum of 512 words of program memory. When selecting a program address value, the MSB of the address is written to the PMADRH register and the LSB is written to the PMADRL register.

9.1.1 PMCON1 AND PMCON2 REGISTERS

PMCON1 is the control register for Flash program memory accesses.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set, in software. They are cleared by hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write operation to occur. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a Reset during normal operation. In these situations, following Reset, the user can check the WRERR bit and execute the appropriate error handling routine.

The PMCON2 register is a write-only register. Attempting to read the PMCON2 register will return all '0's.

To enable writes to the program memory, a specific pattern (the unlock sequence), must be written to the PMCON2 register. The required unlock sequence prevents inadvertent writes to the program memory write latches and Flash program memory.

9.2 Flash Program Memory Overview

It is important to understand the Flash program memory structure for erase and programming operations. Flash program memory is arranged in rows. A row consists of a fixed number of 14-bit program memory words. A row is the minimum size that can be erased by user software.

After a row has been erased, the user can reprogram all or a portion of this row. Data to be written into the program memory row is written to 14-bit wide data write latches. These write latches are not directly accessible to the user, but may be loaded via sequential writes to the PMDATH:PMDATL register pair.

Note: If the user wants to modify only a portion of a previously programmed row, then the contents of the entire row must be read and saved in RAM prior to the erase. Then, new data and retained data can be written into the write latches to reprogram the row of Flash program memory. However, any unprogrammed locations can be written without first erasing the row. In this case, it is not necessary to save and rewrite the other previously programmed locations.

See Table 9-1 for Erase Row size and the number of write latches for Flash program memory.
9.2.1 READING THE FLASH PROGRAM MEMORY

To read a program memory location, the user must:

1. Write the desired address to the PMADRH:PMADRL register pair.
2. Clear the CFGS bit of the PMCON1 register.
3. Then, set control bit RD of the PMCON1 register.

Once the read control bit is set, the program memory Flash controller will use the second instruction cycle to read the data. This causes the second instruction immediately following the “BSF PMCON1,RD” instruction to be ignored. The data is available in the very next cycle, in the PMDATH:PMDATL register pair; therefore, it can be read as two bytes in the following instructions.

PMDATH:PMDATL register pair will hold this value until another read or until it is written to by the user.

**Note:** The two instructions following a program memory read are required to be NOPs. This prevents the user from executing a 2-cycle instruction on the next instruction after the RD bit is set.

### TABLE 9-1: FLASH MEMORY ORGANIZATION BY DEVICE

<table>
<thead>
<tr>
<th>Device</th>
<th>Row Erase (words)</th>
<th>Write Latches (words)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC10(L)F320</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>PIC10(L)F322</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### FIGURE 9-1: FLASH PROGRAM MEMORY READ FLOWCHART
EXAMPLE 9-1: FLASH PROGRAM MEMORY READ

* This code block will read 1 word of program memory at the memory address:
  * PROG_ADDR_HI: PROG_ADDR_LO
  * data will be returned in the variables;
  * PROG_DATA_HI, PROG_DATA_LO

BANKSEL PMADRL ; not required on devices with 1 Bank of SFRs
MOVLW PROG_ADDR_LO ;
MOVWF PMADRL ; Store LSB of address
MOVLW PROG_ADDR_HI ;
MOVWF PMADRHI ; Store MSB of address
BCF PMCON1,CFGS ; Do not select Configuration Space
BSF PMCON1,RD ; Initiate read
NOP ; Ignored (Figure 9-2)
NOP ; Ignored (Figure 9-2)
MOVF PMDATL,W ; Get LSB of word
MOVWF PROG_DATA_LO ; Store in user location
MOVF PMDATH,W ; Get MSB of word
MOVWF PROG_DATA_HI ; Store in user location
9.2.2  FLASH MEMORY UNLOCK SEQUENCE

The unlock sequence is a mechanism that protects the Flash program memory from unintended self-write programming or erasing. The sequence must be executed and completed without interruption to successfully complete any of the following operations:

- Row Erase
- Load program memory write latches
- Write of program memory write latches to program memory
- Write of program memory write latches to User IDs

The unlock sequence consists of the following steps:

1. Write 55h to PMCON2
2. Write AAh to PMCON2
3. Set the WR bit in PMCON1
4. NOP instruction
5. NOP instruction

Once the WR bit is set, the processor will always force two NOP instructions. When an Erase Row or Program Row operation is being performed, the processor will stall internal operations (typical 2 ms), until the operation is complete and then resume with the next instruction. When the operation is loading the program memory write latches, the processor will always force the two NOP instructions and continue uninterrupted with the next instruction.

Since the unlock sequence must not be interrupted, global interrupts should be disabled prior to the unlock sequence and re-enabled after the unlock sequence is completed.

Note: A delay of at least 100 μs is required after Power-On Reset (POR) before executing a Flash memory unlock sequence.

Figure 9-3: FLASH PROGRAM MEMORY UNLOCK SEQUENCE FLOWCHART

Start Unlock Sequence

Write 055h to PMCON2

Write 0AAh to PMCON2

Initiate Write or Erase operation (WR = 1)

Instruction Fetched ignored
NOP execution forced

Instruction Fetched ignored
NOP execution forced

End Unlock Sequence
9.2.3 ERASING FLASH PROGRAM MEMORY

While executing code, program memory can only be erased by rows. To erase a row:

1. Load the PMADRH:PMADRL register pair with any address within the row to be erased.
2. Clear the CFGS bit of the PMCON1 register.
3. Set the FREE and WREN bits of the PMCON1 register.
4. Write 55h, then AAh, to PMCON2 (Flash programming unlock sequence).
5. Set control bit WR of the PMCON1 register to begin the erase operation.

See Example 9-2.

After the "BSF PMCON1, WR" instruction, the processor requires two cycles to set up the erase operation. The user must place two NOP instructions after the WR bit is set. The processor will halt internal operations for the typical 2 ms erase time. This is not Sleep mode as the clocks and peripherals will continue to run. After the erase cycle, the processor will resume operation with the third instruction after the PMCON1 write instruction.

![Flash Program Memory Erase Flowchart](image-url)
EXAMPLE 9-2: ERASING ONE ROW OF PROGRAM MEMORY

; This row erase routine assumes the following:
; 1. A valid address within the erase row is loaded in ADDRH:ADDRL
; 2. ADDRH and ADDRL are located in shared data memory 0x70 - 0x7F (common RAM)

BCF INTCON,GIE ; Disable ints so required sequences will execute properly
BANKSEL PMADRL ; not required on devices with 1 Bank of SFRs
MOVF ADDRL,W ; Load lower 8 bits of erase address boundary
MOVWF PMADRL
MOVF ADDRH,W ; Load upper 6 bits of erase address boundary
MOVWF PMADRH
BCF PMCON1,CFGS ; Not configuration space
BSF PMCON1,FREE ; Specify an erase operation
BSF PMCON1,WREN ; Enable writes

MOVLW 55h ; Start of required sequence to initiate erase
MOVWF PMCON2 ; Write 55h
MOVLW 0AAh ;
MOVWF PMCON2 ; Write AAh
BSF PMCON1,WR ; Set WR bit to begin erase
NOP ; NOP instructions are forced as processor starts
NOP ; row erase of program memory.
; The processor stalls until the erase process is complete
; after erase processor continues with 3rd instruction

BCF PMCON1,WREN ; Disable writes
BSF INTCON,GIE ; Enable interrupts
9.2.4 WRITING TO FLASH PROGRAM MEMORY

Program memory is programmed using the following steps:

1. Load the address in PMADRH:PMADRL of the row to be programmed.
2. Load each write latch with data.
3. Initiate a programming operation.
4. Repeat steps 1 through 3 until all data is written.

Before writing to program memory, the word(s) to be written must be erased or previously unwritten. Program memory can only be erased one row at a time. No automatic erase occurs upon the initiation of the write.

Program memory can be written one or more words at a time. The maximum number of words written at one time is equal to the number of write latches. Program memory can only be erased one row at a time.

The write latches are aligned to the Flash row address boundary defined by the upper ten bits of PMADR:PMADRL, (PMADR<6:0>:PMADRL<7:5>) with the lower five bits of PMADRL, (PMADRL<4:0>) determining the write latch being loaded. Write operations do not cross these boundaries. At the completion of a program memory write operation, the data in the write latches is reset to contain 0x3FFF.

The following steps should be completed to load the write latches and program a row of program memory. These steps are divided into two parts. First, each write latch is loaded with data from the PMDATH:PMDATL using the unlock sequence with LWLO = 1. When the last word to be loaded into the write latch is ready, the LWLO bit is cleared and the unlock sequence executed. This initiates the programming operation, writing all the latches into Flash program memory.

Note: The special unlock sequence is required to load a write latch with data or initiate a Flash programming operation. If the unlock sequence is interrupted, writing to the latches or program memory will not be initiated.

1. Set the WREN bit of the PMCON1 register.
2. Clear the CFGS bit of the PMCON1 register.
3. Set the LWLO bit of the PMCON1 register. When the LWLO bit of the PMCON1 register is ‘1’, the write sequence will only load the write latches and will not initiate the write to Flash program memory.
4. Load the PMADRH:PMADRL register pair with the address of the location to be written.
5. Load the PMDATH:PMDATL register pair with the program memory data to be written.
6. Execute the unlock sequence (Section 9.2.2 “Flash Memory Unlock Sequence”). The write latch is now loaded.
7. Increment the PMADRH:PMADRL register pair to point to the next location.
8. Repeat steps 5 through 7 until all but the last write latch has been loaded.
9. Clear the LWLO bit of the PMCON1 register. When the LWLO bit of the PMCON1 register is ‘0’, the write sequence will initiate the write to Flash program memory.
10. Load the PMDATH:PMDATL register pair with the program memory data to be written.
11. Execute the unlock sequence (Section 9.2.2 “Flash Memory Unlock Sequence”). The entire program memory latch content is now written to Flash program memory.

Note: The program memory write latches are reset to the blank state (0x3FFF) at the completion of every write or erase operation. As a result, it is not necessary to load all the program memory write latches. Unloaded latches will remain in the blank state.

An example of the complete write sequence is shown in Example 9-3. The initial address is loaded into the PMADRH:PMADRL register pair; the data is loaded using indirect addressing.
FIGURE 9-5: BLOCK WRITES TO FLASH PROGRAM MEMORY WITH 16 WRITE LATCHES

Program Memory Write Latches

<table>
<thead>
<tr>
<th>Row</th>
<th>Addr</th>
<th>Addr</th>
<th>Addr</th>
<th>Addr</th>
</tr>
</thead>
<tbody>
<tr>
<td>000h</td>
<td>0000h</td>
<td>0001h</td>
<td>000Eh</td>
<td>000Fh</td>
</tr>
<tr>
<td>001h</td>
<td>0010h</td>
<td>0011h</td>
<td>001Eh</td>
<td>001Fh</td>
</tr>
<tr>
<td>002h</td>
<td>0020h</td>
<td>0021h</td>
<td>002Eh</td>
<td>002Fh</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>01Eh</td>
<td>01E0h</td>
<td>01E1h</td>
<td>01EEh</td>
<td>01EFh</td>
</tr>
<tr>
<td>01Fh</td>
<td>01F0h</td>
<td>01F1h</td>
<td>01FEh</td>
<td>01FFh</td>
</tr>
</tbody>
</table>

Flash Program Memory

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>USER ID 0 - 3</td>
<td>reserved</td>
<td>DEVICEID</td>
<td>REVID</td>
<td>Configuration Word</td>
<td>reserved</td>
</tr>
</tbody>
</table>

Configuration Memory

- CFGS = 0
- CFGS = 1
FIGURE 9-6: FLASH PROGRAM MEMORY WRITE FLOWCHART

1. Start Write Operation
2. Determine number of words to be written into Program or Configuration Memory. The number of words cannot exceed the number of words per row. (word_cnt)
3. Disable Interrupts (GIE = 0)
4. Select Program or Config. Memory (CFGS)
5. Select Row Address (PMADRH:PMADRL)
6. Select Write Operation (FREE = 0)
7. Load Write Latches Only (LWLO = 1)
8. Enable Write/Erase Operation (WREN = 1)
9. Load the value to write (PMDATH:PMDATL)
10. Update the word counter (word_cnt--)
11. Last word to write? Yes
12. Unlock Sequence Figure 9-3
13. No delay when writing to Program Memory Latches
14. Increment Address (PMADRH:PMADRL++)
15. No
16. Unlock Sequence Figure 9-3
17. Write Latches to Flash (LWLO = 0)
18. CPU stalls while Write operation completes (2ms typical)
19. Disable Write/Erase Operation (WREN = 0)
20. Re-enable Interrupts (GIE = 1)
21. End Write Operation
EXAMPLE 9-3: WRITING TO FLASH PROGRAM MEMORY

; This write routine assumes the following:
; A valid starting address (the least significant bits = '00')
; is loaded in ADDRH:ADDRL
; ADDRH, ADDRL and DATADDR are all located in data memory

; BANKSEL PMADRH
MOVF ADDRH,W ;Load initial address
MOVWF PMADRH ;
MOVF ADDRL,W ;
MOVWF PMADRL ;
MOVF DATADDR,W ;Load initial data address
MOVWF FSR ;
LOOP MOVF INDF,W ;Load first data byte into lower
MOVWF PMDATL ;
INC FSR,F ;Next byte
MOVF INDF,W ;Load second data byte into upper
MOVWF PMDATH ;
INC FSR,F ;
BANKSEL PMCON1
BSF PMCON1,WREN ;Enable writes
BCF INTCON,GIE ;Disable interrupts (if using)
BTFSC INTCON,GIE ;See AN576
GOTO $-2

; Required Sequence
MOVLW 55h ;Start of required write sequence:
MOVWF PMCON2 ;Write 55h
MOVLW 0AAh ;
MOVWF PMCON2 ;Write 0AAh
BSF PMCON1,WR ;Set WR bit to begin write
NOP ;Required to transfer data to the buffer
NOP ;registers

; Required to transfer data to the buffer
BCF PMCON1,WREN ;Disable writes
BSF INTCON,GIE ;Enable interrupts (comment out if not using interrupts)
BANKSEL PMADRL
MOVF PMADRL,F ;Increment address
ANDLW 0x03 ;Indicates when sixteen words have been programmed
SUBLW 0x03 ;Change value for different size write blocks
; 0x0F = 16 words
; 0x0B = 12 words
; 0x07 = 8 words
; 0x03 = 4 words
BTFSS STATUS,Z ;Exit on a match,
GOTO LOOP ;Continue if more data needs to be written
9.3 Modifying Flash Program Memory

When modifying existing data in a program memory row, and data within that row must be preserved, it must first be read and saved in a RAM image. Program memory is modified using the following steps:

1. Load the starting address of the row to be modified.
2. Read the existing data from the row into a RAM image.
3. Modify the RAM image to contain the new data to be written into program memory.
4. Load the starting address of the row to be rewritten.
5. Erase the program memory row.
6. Load the write latches with data from the RAM image.
7. Initiate a programming operation.

FIGURE 9-7: FLASH PROGRAM MEMORY MODIFY FLOWCHART

- **Start**
- **Modify Operation**
- **Read Operation**
  - Figure 9-2
- **An image of the entire row read must be stored in RAM**
- **Modify Image**
  - The words to be modified are changed in the RAM image
- **Erase Operation**
  - Figure 9-4
- **Write Operation**
  - Use RAM image
  - Figure 9-5
- **End**
- **Modify Operation**
9.4 User ID, Device ID and Configuration Word Access

Instead of accessing program memory, the User ID's, Device ID/Revision ID and Configuration Word can be accessed when CFGS = 1 in the PMCON1 register. This is the region that would be pointed to by PC<13> = 1, but not all addresses are accessible. Different access may exist for reads and writes. Refer to Table 9-2.

When read access is initiated on an address outside the parameters listed in Table 9-2, the PMDATL:PMDATL register pair is cleared, reading back '0's.

| TABLE 9-2: USER ID, DEVICE ID AND CONFIGURATION WORD ACCESS (CFGS = 1) |
|----------------|----------------|----------------|
| Address        | Function        | Read Access    | Write Access |
| 2000h-2003h    | User IDs        | Yes            | Yes          |
| 2006h          | Device ID/Revision ID | Yes | No |
| 2007h          | Configuration Word | Yes | No |

EXAMPLE 9-4: CONFIGURATION WORD AND DEVICE ID ACCESS

* This code block will read 1 word of program memory at the memory address:
* PROG_ADDR_LO (must be 00h-08h) data will be returned in the variables;
* PROG_DATA_HI, PROG_DATA_LO

```
BANKSEL PMADRL ; not required on devices with 1 Bank of SFRs
MOVWF PMADDRL ; Store LSB of address
CLRF PMADRH ; Clear MSB of address

BSF PMCON1,CFGS ; Select Configuration Space
BCF INTCON,GIE ; Disable interrupts
BSF PMCON1,RD ; Initiate read
NOP ; Executed (See Figure 9-2)
NOP ; Ignored (See Figure 9-2)
BSF INTCON,GIE ; Restore interrupts

MOVF PMDATL,W ; Get LSB of word
MOVF PMDATL,W ; Store in user location
MOVF PMDATL,W ; Get MSB of word
MOVF PMDATL,W ; Store in user location
```
9.5 Write Verify

It is considered good programming practice to verify that program memory writes agree with the intended value. Since program memory is stored as a full page then the stored program memory contents are compared with the intended data stored in RAM after the last write is complete.

FIGURE 9-8: FLASH PROGRAM MEMORY VERIFY FLOWCHART

This routine assumes that the last row of data written was from an image saved in RAM. This image will be used to verify the data currently stored in Flash Program Memory.

Read Operation

PMDAT = RAM image?

Yes

Fail Verify Operation

Last Word?

No

Yes

End Verify Operation

No
9.6 Flash Program Memory Control Registers

REGISTER 9-1: PMDATL: PROGRAM MEMORY DATA LOW

<table>
<thead>
<tr>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>PMDAT&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as '0'

u = Bit is unchanged  
x = Bit is unknown  
-\text{n}/n = Value at POR and BOR/Value at all other Resets

‘1’ = Bit is set  
‘0’ = Bit is cleared

bit 7-0  
PMDAT<7:0>: The value of the program memory word pointed to by PMADRH and PMADRL after a Program Memory Read command.

REGISTER 9-2: PMDATH: PROGRAM MEMORY DATA HIGH

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>PMDAT&lt;13:8&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as ‘0’

u = Bit is unchanged  
x = Bit is unknown  
-\text{n}/n = Value at POR and BOR/Value at all other Resets

‘1’ = Bit is set  
‘0’ = Bit is cleared

bit 7-6  
Unimplemented: Read as ‘0’

bit 5-0  
PMDAT<13:8>: The value of the program memory word pointed to by PMADRH and PMADRL after a Program Memory Read command.
### REGISTER 9-3: PMADRL: PROGRAM MEMORY ADDRESS LOW

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMADR&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

**bit 7-0**: PMADR<7:0>: Program Memory Read Address low bits

### REGISTER 9-4: PMADRH: PROGRAM MEMORY ADDRESS HIGH

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PMADR8</td>
</tr>
</tbody>
</table>

#### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

**bit 7**: PMADRH: Program Memory Read Address High bit

**bit 7-1**: Unimplemented: Read as '0'

**bit 0**: PMADR8: Program Memory Read Address High bit
## REGISTER 9-5: PMCON1: PROGRAM MEMORY CONTROL 1 REGISTER

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6</th>
<th>bit 5</th>
<th>bit 4</th>
<th>bit 3</th>
<th>bit 2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CFGS</td>
<td>LWLO</td>
<td>FREE</td>
<td>WRERR</td>
<td>WREN</td>
<td>WR</td>
<td>RD</td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- S = Bit can only be set
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- HC = Bit is cleared by hardware

### Bit 7
**Unimplemented**: Read as ‘1’

### Bit 6
**CFGS**: Configuration Select bit
- 1 = Access Configuration, User ID and Device ID Registers
- 0 = Access Flash program memory

### Bit 5
**LWLO**: Load Write Latches Only bit
- 1 = Only the addressed program memory write latch is loaded/updated on the next WR command
- 0 = The addressed program memory write latch is loaded/updated and a write of all program memory write latches will be initiated on the next WR command

### Bit 4
**FREE**: Program Flash Erase Enable bit
- 1 = Performs an erase operation on the next WR command (hardware cleared upon completion)
- 0 = Performs an write operation on the next WR command

### Bit 3
**WRERR**: Program/Erase Error Flag bit
- 1 = Condition indicates an improper program or erase sequence attempt or termination (bit is set automatically on any set attempt (write ‘1’) of the WR bit).
- 0 = The program or erase operation completed normally.

### Bit 2
**WREN**: Program/Erase Enable bit
- 1 = Allows program/erase cycles
- 0 = Inhibits programming/erasing of program Flash

### Bit 1
**WR**: Write Control bit
- 1 = Initiates a program Flash program/erase operation.
  - The operation is self-timed and the bit is cleared by hardware once operation is complete.
  - The WR bit can only be set (not cleared) in software.
- 0 = Program/erase operation to the Flash is complete and inactive.

### Bit 0
**RD**: Read Control bit
- 1 = Initiates a program Flash read. Read takes one cycle. RD is cleared in hardware. The RD bit can only be set (not cleared) in software.
- 0 = Does not initiate a program Flash read.

**Note 1**: Unimplemented bit, read as ‘1’.

**Note 2**: The WRERR bit is automatically set by hardware when a program memory write or erase operation is started (WR = 1).

**Note 3**: The LWLO bit is ignored during a program memory erase operation (FREE = 1).
### REGISTER 9-6: PMCON2: PROGRAM MEMORY CONTROL 2 REGISTER

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>W-0/0</td>
<td>W-0/0</td>
<td>W-0/0</td>
<td>W-0/0</td>
<td>W-0/0</td>
<td>W-0/0</td>
<td>W-0/0</td>
<td>W-0/0</td>
</tr>
</tbody>
</table>

Program Memory Control Register 2

#### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **S** = Bit can only be set
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

#### bit 7-0 Flash Memory Unlock Pattern bits
To unlock writes, a 55h must be written first, followed by an AAh, before setting the WR bit of the PMCON1 register. The value written to this register is used to unlock the writes. There are specific timing requirements on these writes.

### TABLE 9-3: SUMMARY OF REGISTERS ASSOCIATED WITH FLASH PROGRAM MEMORY

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTCON</td>
<td><strong>GIE</strong></td>
<td><strong>PEIE</strong></td>
<td><strong>TMR0IE</strong></td>
<td><strong>INTE</strong></td>
<td><strong>IOCIE</strong></td>
<td><strong>TMR0IF</strong></td>
<td><strong>INTF</strong></td>
<td><strong>IOCIF</strong></td>
<td>40</td>
</tr>
<tr>
<td>PMCON1</td>
<td>—</td>
<td><strong>CFGs</strong></td>
<td><strong>LWLO</strong></td>
<td><strong>FREE</strong></td>
<td><strong>WRERR</strong></td>
<td><strong>WREN</strong></td>
<td><strong>WR</strong></td>
<td><strong>RD</strong></td>
<td>65</td>
</tr>
<tr>
<td>PMCON2</td>
<td>Program Memory Control Register 2</td>
<td>66</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PMADRL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>PMADRH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>PMDATL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>PMDATH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

#### Legend:
- — = unimplemented location, read as '0'. Shaded cells are not used by Flash program memory module.

### TABLE 9-4: SUMMARY OF CONFIGURATION WORD WITH FLASH PROGRAM MEMORY

<table>
<thead>
<tr>
<th>Name</th>
<th>Bits</th>
<th>Bit -7</th>
<th>Bit -6</th>
<th>Bit 13/5</th>
<th>Bit 12/4</th>
<th>Bit 11/3</th>
<th>Bit 10/2</th>
<th>Bit 9/1</th>
<th>Bit 8/0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>CONFIG</td>
<td>13:8</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td><strong>WRT&lt;1:0&gt;</strong></td>
<td><strong>BORV</strong></td>
<td><strong>LPBOR</strong></td>
<td><strong>LVP</strong></td>
<td>20</td>
<td></td>
</tr>
<tr>
<td></td>
<td>7:0</td>
<td><strong>CP</strong></td>
<td><strong>MCLR</strong></td>
<td><strong>PWRTIE</strong></td>
<td><strong>WDTE&lt;1:0&gt;</strong></td>
<td><strong>BOREN&lt;1:0&gt;</strong></td>
<td><strong>FOSC</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Legend:
- — = unimplemented location, read as '0'. Shaded cells are not used by Flash program memory.
10.0 I/O PORT

Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled on a port pin, that pin cannot be used as a general purpose output. However, the pin can still be read.

PORTA has three standard registers for its operation. These registers are:

- TRISA register (data direction)
- PORTA register (reads the levels on the pins of the device)
- LATA register (output latch)

Some ports may have one or more of the following additional registers. These registers are:

- ANSELA (analog select)
- WPUA (weak pull-up)

The Data Latch (LATA register) is useful for read-modify-write operations on the value that the I/O pins are driving.

A write operation to the LATA register has the same effect as a write to the corresponding PORTA register. A read of the LATA register reads of the values held in the I/O PORT latches, while a read of the PORTA register reads the actual I/O pin value.

Ports that support analog inputs have an associated ANSELA register. When an ANSEL bit is set, the digital input buffer associated with that bit is disabled. Disabling the input buffer prevents analog signal levels on the pin between a logic high and low from causing excessive current in the logic input circuitry. A simplified model of a generic I/O port, without the interfaces to other peripherals, is shown in Figure 10-1.

EXAMPLE 10-1: INITIALIZING PORTA

```assembly
; This code example illustrates
; initializing the PORTA register. The
; other ports are initialized in the same
; manner.
BANKSEL PORTA ;not required on devices with 1 Bank of SFRs
CLRF PORTA ;Init PORTA
BANKSEL LATA ;not required on devices with 1 Bank of SFRs
CLRF LATA ;
BANKSEL ANSELA ;not required on devices with 1 Bank of SFRs
CLRF ANSELA ;digital I/O
BANKSEL TRISA ;not required on devices with 1 Bank of SFRs
MOVLW B'00000011' ;Set RA<1:0> as inputs
MOVF TRISA ;and set RA<2:3> as
;outputs
```

FIGURE 10-1: I/O PORT OPERATION
10.1 PORTA Registers

PORTA is a 8-bit wide, bidirectional port. The corresponding data direction register is TRISA (Register 10-2). Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., disable the output driver). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., enables output driver and puts the contents of the output latch on the selected pin). Example 10-1 shows how to initialize PORTA.

Reading the PORTA register (Register 10-1) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATA).

The TRISA register (Register 10-2) controls the PORTA pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISA register are maintained set when using them as analog inputs. I/O pins configured as analog input always read ‘0’.

10.1.1 WEAK PULL-UPS

Each of the PORTA pins has an individually configurable internal weak pull-up. Control bits WPUA<3:0> enable or disable each pull-up (see Register 10-5). Each weak pull-up is automatically turned off when the port pin is configured as an output. All pull-ups are disabled on a Power-on Reset by the WPUEN bit of the OPTION_REG register.

10.1.2 ANSELA REGISTER

The ANSELA register (Register 10-4) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELA bit high will cause all digital reads on the pin to be read as ‘0’ and allow analog functions on the pin to operate correctly.

The state of the ANSELA bits has no effect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note: The ANSELA bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to ‘0’ by user software.

10.1.3 PORTA FUNCTIONS AND OUTPUT PRIORITIES

Each PORTA pin is multiplexed with other functions. The pins, their combined functions and their output priorities are shown in Table 10-1.

When multiple outputs are enabled, the actual pin control goes to the peripheral with the highest priority.

Digital output functions may control the pin when it is in Analog mode with the priority shown in Table 10-1.

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Function Priority(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RA0</td>
<td>ICSPDAT</td>
</tr>
<tr>
<td></td>
<td>PWM1</td>
</tr>
<tr>
<td></td>
<td>RA0</td>
</tr>
<tr>
<td>RA1</td>
<td>CWG1B</td>
</tr>
<tr>
<td></td>
<td>PWM2</td>
</tr>
<tr>
<td></td>
<td>CLC1</td>
</tr>
<tr>
<td></td>
<td>RA1</td>
</tr>
<tr>
<td>RA2</td>
<td>NCO1</td>
</tr>
<tr>
<td></td>
<td>CLKR</td>
</tr>
<tr>
<td></td>
<td>RA2</td>
</tr>
<tr>
<td>RA3</td>
<td>None</td>
</tr>
</tbody>
</table>

Note 1: Priority listed from highest to lowest.
10.2 Register Definitions: PORTA

**REGISTER 10-1: PORTA: PORTA REGISTER**

<table>
<thead>
<tr>
<th>bit 7-4</th>
<th>RA3</th>
<th>RA2</th>
<th>RA1</th>
<th>RA0</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>R-x/x</td>
</tr>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>R/W-x/x</td>
</tr>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>R/W-x/x</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

**Note 1:** Writes to PORTx are actually written to the corresponding LATx register. Reads from PORTx register return actual I/O pin values.

**REGISTER 10-2: TRISA: PORTA TRI-STATE REGISTER**

<table>
<thead>
<tr>
<th>bit 7-4</th>
<th>TRISA2</th>
<th>TRISA1</th>
<th>TRISA0</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-1</td>
</tr>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
</tr>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>R/W-1/1</td>
</tr>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>R/W-1/1</td>
</tr>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>R/W-1/1</td>
</tr>
<tr>
<td>TRISA2</td>
<td>TRISA1</td>
<td>TRISA0</td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

**Note 1:** Unimplemented, read as '1'.
## REGISTER 10-3:  LATA: PORTA DATA LATCH REGISTER

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>LATA2</td>
<td>LATA1</td>
<td>LATA0</td>
</tr>
</tbody>
</table>

| bit 7 | bit 0 |

### Legend:
- **R** = Readable bit  
- **W** = Writable bit  
- **U** = Unimplemented bit, read as ‘0’  
- **u** = Bit is unchanged  
- **x** = Bit is unknown  
- **-n/n** = Value at POR and BOR/Value at all other Resets  
- ‘1’ = Bit is set  
- ‘0’ = Bit is cleared

- **Unimplemented**: Read as ‘0’.
- **LATA<2:0>**: RA<2:0> Output Latch Value bits

### Note 1:
Writes to PORTx are actually written to the corresponding LATx register. Reads from LATx register return register values, not I/O pin values.

## REGISTER 10-4:  ANSELA: PORTA ANALOG SELECT REGISTER

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>ANSA2</td>
<td>ANSA1</td>
<td>ANSA0</td>
</tr>
</tbody>
</table>

| bit 7 | bit 0 |

### Legend:
- **R** = Readable bit  
- **W** = Writable bit  
- **U** = Unimplemented bit, read as ‘0’  
- **u** = Bit is unchanged  
- **x** = Bit is unknown  
- **-n/n** = Value at POR and BOR/Value at all other Resets  
- ‘1’ = Bit is set  
- ‘0’ = Bit is cleared

- **Unimplemented**: Read as ‘0’.
- **ANSA<2:0>**: Analog Select between Analog or Digital Function on Pins RA<2:0>, respectively  
  - **1** = Analog input. Pin is assigned as analog input(1). Digital Input buffer disabled.  
  - **0** = Digital I/O. Pin is assigned to port or Digital special function.

### Note 1:
Setting a pin to an analog input automatically disables the digital input circuitry. Weak pull-ups, if available, are unaffected. The corresponding TRIS bit must be set to Input mode by the user in order to allow external control of the voltage on the pin.
REGISTER 10-5:  WPUA: WEAK PULL-UP PORTA REGISTER

| bit 7-4 | Unimplemented: Read as '0'. |
| bit 3-0 | WPUA<3:0>: Weak Pull-up PORTA Control bits |

  - 1 = Weak Pull-up enabled(1)
  - 0 = Weak Pull-up disabled.

**Note 1:** Enabling weak pull-ups also requires that the WPUEN bit of the OPTION_REG register be cleared *(Register 16-1).*
## TABLE 10-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANSELA</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ANSA2</td>
<td>ANSA1</td>
<td>ANSA0</td>
</tr>
<tr>
<td>IOCAF</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>IOCAF3</td>
<td>IOCAF2</td>
<td>IOCAF1</td>
</tr>
<tr>
<td>IOCAN</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>IOCAN3</td>
<td>IOCAN2</td>
<td>IOCAN1</td>
</tr>
<tr>
<td>IOCAP</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>IOCAP3</td>
<td>IOCAP2</td>
<td>IOCAP1</td>
</tr>
<tr>
<td>LATA</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>LATA2</td>
<td>LATA1</td>
</tr>
<tr>
<td>PORTA</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>RA3</td>
<td>RA2</td>
<td>RA1</td>
<td>RA0</td>
</tr>
<tr>
<td>TRISA</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TRISA2</td>
<td>TRISA1</td>
<td>TRISA0</td>
</tr>
<tr>
<td>WPUA</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>WPUA3</td>
<td>WPUA2</td>
<td>WPUA1</td>
</tr>
</tbody>
</table>

**Legend:**
- x = unknown, u = unchanged, – = unimplemented locations read as ‘0’. Shaded cells are not used by PORTA.

**Note 1:** Unimplemented, read as ‘1’.
11.0 INTERRUPT-ON-CHANGE

The PORTA pins can be configured to operate as Interrupt-On-Change (IOC) pins. An interrupt can be generated by detecting a signal that has either a rising edge or a falling edge. Any individual PORTA pin, or combination of PORTA pins, can be configured to generate an interrupt. The Interrupt-on-change module has the following features:

- Interrupt-on-Change enable (Master Switch)
- Individual pin configuration
- Rising and falling edge detection
- Individual pin interrupt flags

Figure 11-1 is a block diagram of the IOC module.

11.1 Enabling the Module

To allow individual PORTA pins to generate an interrupt, the IOCIE bit of the INTCON register must be set. If the IOCIE bit is disabled, the edge detection on the pin will still occur, but an interrupt will not be generated.

11.2 Individual Pin Configuration

For each PORTA pin, a rising edge detector and a falling edge detector are present. To enable a pin to detect a rising edge, the associated IOCAPx bit of the IOCAP register is set. To enable a pin to detect a falling edge, the associated IOCANx bit of the IOCAN register is set.

A pin can be configured to detect rising and falling edges simultaneously by setting both the IOCAPx bit and the IOCANx bit of the IOCAP and IOCAN registers, respectively.

11.3 Interrupt Flags

The IOCAFx bits located in the IOCAF register are status flags that correspond to the interrupt-on-change pins of PORTA. If an expected edge is detected on an appropriately enabled pin, then the status flag for that pin will be set, and an interrupt will be generated if the IOCIE bit is set. The IO CIF bit of the INTCON register reflects the status of all IOCAFx bits.

11.4 Clearing Interrupt Flags

The individual status flags, (IOCAFx bits), can be cleared by resetting them to zero. If another edge is detected during this clearing operation, the associated status flag will be set at the end of the sequence, regardless of the value actually being written.

In order to ensure that no detected edge is lost while clearing flags, only AND operations masking out known changed bits should be performed. The following sequence is an example of what should be performed.

**EXAMPLE 11-1: CLEARING INTERRUPT FLAGS**

```
MOVLW 0xff
XORWF IOCAF, W
ANDWF IOCAF, F
```

11.5 Operation in Sleep

The interrupt-on-change interrupt sequence will wake the device from Sleep mode, if the IOCIE bit is set.

If an edge is detected while in Sleep mode, the IOCAF register will be updated prior to the first instruction executed out of Sleep.
FIGURE 11-1: INTERRUPT-ON-CHANGE BLOCK DIAGRAM

Data Bus = 0 or 1

From all other IOCAFx individual pin detectors

Q1  Q1
Q2  Q2
Q3  Q3

IOC Interrupt to CPU Core

To Data Bus IOCAFx

Write IOCAFx

Edge Detect

Q4Q1

RAx

IOCAPx

Q2

IOCANx

DCK

DCK

D CK

S CK

R R

Q3

Q1

Q2

Q3

Q1

Q2

Q3

Q1

Q2

Q3

Q1

Q2

Q3

Q1

Q2

Q3

Q1

Q2

Q3
11.6 Interrupt-On-Change Registers

REGISTER 11-1: IOCAP: INTERRUPT-ON-CHANGE PORTA POSITIVE EDGE REGISTER

| bit 7-4 | Unimplemented: Read as ‘0’. |
| bit 3-0 | IOCAP<3:0>: Interrupt-on-Change PORTA Positive Edge Enable bits |
| 1      | Interrupt-on-Change enabled on the pin for a positive going edge. Associated Status bit and interrupt flag will be set upon detecting an edge. |
| 0      | Interrupt-on-Change disabled for the associated pin. |

Note 1: Interrupt-on-change also requires that the IOCIE bit of the INTCON register be set (Register 6-1).

REGISTER 11-2: IOCAN: INTERRUPT-ON-CHANGE PORTA NEGATIVE EDGE REGISTER

| bit 7-4 | Unimplemented: Read as ‘0’. |
| bit 3-0 | IOCAN<3:0>: Interrupt-on-Change PORTA Negative Edge Enable bits |
| 1      | Interrupt-on-Change enabled on the pin for a negative going edge. Associated Status bit and interrupt flag will be set upon detecting an edge. |
| 0      | Interrupt-on-Change disabled for the associated pin. |

Note 1: Interrupt-on-change also requires that the IOCIE bit of the INTCON register be set (Register 6-1).
### TABLE 11-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPT-ON-CHANGE

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTCON</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>40</td>
</tr>
<tr>
<td>IOCAF</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>76</td>
</tr>
<tr>
<td>IOCAN</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>75</td>
</tr>
<tr>
<td>IOCAP</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>75</td>
</tr>
<tr>
<td>TRISA</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>_</td>
<td>_</td>
<td>69</td>
</tr>
</tbody>
</table>

**Legend:** — = unimplemented location, read as ‘0’. Shaded cells are not used by Interrupt-on-Change.

**Note 1:** Unimplemented, read as ‘1’.

---

**REGISTER 11-3:** IOCAF: INTERRUPT-ON-CHANGE PORTA FLAG REGISTER

<table>
<thead>
<tr>
<th>Bit 7-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>IOCAF3</td>
<td>IOCAF2</td>
<td>IOCAF1</td>
<td>IOCAF0</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- x = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- HS = Bit is set in hardware
- u = Bit is unchanged
- -n/n = Value at POR and BOR/Value at all other Resets

**Legend:**

- Unimplemented: Read as ‘0’.

**bit 7-4** Unimplemented: Read as ‘0’.

**bit 3-0** ICAF<3:0>: Interrupt-on-Change PORTA Flag bits

- 1 = An enable change was detected on the associated pin.
  - Set when IOCAPx = 1 and a rising edge was detected on RAx, or when IOCANx = 1 and a falling edge was detected on RAx.(1)
- 0 = No change was detected, or the user cleared the detected change.

**Note 1:** Interrupt-on-change also requires that the IOCIE bit of the INTCON register be set (Register 6-1).
12.0 FIXED VOLTAGE REFERENCE (FVR)

The Fixed Voltage Reference, or FVR, is a stable voltage reference, independent of VDD, with 1.024V, 2.048V or 4.096V selectable output levels. The output of the FVR can be configured to supply a reference voltage to the following:

- ADC input channel

The FVR can be enabled by setting the FVREN bit of the FVRCON register.

12.1 Independent Gain Amplifiers

The output of the FVR supplied to the ADC is routed through an independent programmable gain amplifier. The amplifier can be configured to amplify the reference voltage by 1x, 2x or 4x, to produce the three possible voltage levels.

The ADFVR<1:0> bits of the FVRCON register are used to enable and configure the gain amplifier settings for the reference supplied to the ADC module. Reference Section 15.0 “Analog-to-Digital Converter (ADC) Module” for additional information.

To minimize current consumption when the FVR is disabled, the FVR buffers should be turned off by clearing the ADFVR<1:0> bits.

12.2 FVR Stabilization Period

When the Fixed Voltage Reference module is enabled, it requires time for the reference and amplifier circuits to stabilize. Once the circuits stabilize and are ready for use, the FVRRDY bit of the FVRCON register will be set. See Section 24.0 “Electrical Specifications” for the minimum delay requirement.

---

**FIGURE 12-1: VOLTAGE REFERENCE BLOCK DIAGRAM**

![Voltage Reference Block Diagram](image)

**TABLE 12-1: PERIPHERALS REQUIRING THE FIXED VOLTAGE REFERENCE (FVR)**

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>Conditions</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>HFINTOSC</td>
<td>FOSC = 1</td>
<td>EC on CLKIN pin.</td>
</tr>
<tr>
<td>BOR</td>
<td>BOREN&lt;1:0&gt; = 11</td>
<td>BOR always enabled.</td>
</tr>
<tr>
<td></td>
<td>BOREN&lt;1:0&gt; = 10 and BORFS = 1</td>
<td>BOR disabled in Sleep mode, BOR Fast Start enabled.</td>
</tr>
<tr>
<td></td>
<td>BOREN&lt;1:0&gt; = 01 and BORFS = 1</td>
<td>BOR under software control, BOR Fast Start enabled.</td>
</tr>
<tr>
<td>IVR</td>
<td>All PIC10F320/322 devices, when VREGPM1 = 1 and not in Sleep</td>
<td>The device runs off of the Power-Save mode regulator when in Sleep mode.</td>
</tr>
</tbody>
</table>
12.3 FVR Control Registers

REGISTER 12-1: FVRCON: FIXED VOLTAGE REFERENCE CONTROL REGISTER

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>FVREN</td>
<td>FVRRDY(1)</td>
<td>TSEN(3)</td>
<td>TSRNG(3)</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ADFVR&lt;1:0&gt;</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
u = Bit is unchanged  x = Bit is unknown  -n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set  ‘0’ = Bit is cleared  q = Value depends on condition

bit 7  
**FVREN:** Fixed Voltage Reference Enable bit
  1 = Fixed Voltage Reference is enabled
  0 = Fixed Voltage Reference is disabled

bit 6  
**FVRRDY:** Fixed Voltage Reference Ready Flag bit(1)
  1 = Fixed Voltage Reference output is ready for use
  0 = Fixed Voltage Reference output is not ready or not enabled

bit 5  
**TSEN:** Temperature Indicator Enable bit(3)
  1 = Temperature Indicator is enabled
  0 = Temperature Indicator is disabled

bit 4  
**TSRNG:** Temperature Indicator Range Selection bit(3)
  1 = VOUT = VDD - 4VT (High Range)
  0 = VOUT = VDD - 2VT (Low Range)

bit 3-2  
Unimplemented: Read as ‘0’

bit 1-0  
**ADFVR<1:0>:** ADC Fixed Voltage Reference Selection bit
  11 = ADC Fixed Voltage Reference Peripheral output is 4x (4.096V)(2)
  10 = ADC Fixed Voltage Reference Peripheral output is 2x (2.048V)(2)
  01 = ADC Fixed Voltage Reference Peripheral output is 1x (1.024V)
  00 = ADC Fixed Voltage Reference Peripheral output is off.

Note 1: FVRRDY indicates the true state of the FVR.
2: Fixed Voltage Reference output cannot exceed VDD.
3: See Section 14.0 “Temperature Indicator Module” for additional information.

TABLE 12-2: SUMMARY OF REGISTERS ASSOCIATED WITH FIXED VOLTAGE REFERENCE

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on page</th>
</tr>
</thead>
<tbody>
<tr>
<td>FVRCON</td>
<td>FVREN</td>
<td>FVRRDY</td>
<td>TSEN</td>
<td>TSRNG</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ADFVR&lt;1:0&gt;</td>
<td>78</td>
</tr>
</tbody>
</table>

Legend: Shaded cells are not used with the Fixed Voltage Reference.
13.0  INTERNAL VOLTAGE REGULATOR (IVR)

The Internal Voltage Regulator (IVR), which provides operation above 3.6V is available on:

- PIC10F320
- PIC10F322

This circuit regulates a voltage for the internal device logic while permitting the VDD and I/O pins to operate at a higher voltage. When VDD approaches the regulated voltage, the IVR output automatically tracks the input voltage.

The IVR operates in one of three power modes based on user configuration and peripheral selection. The operating power modes are:

- High
- Low
- Power-Save Sleep mode

Power modes are selected automatically depending on the device operation, as shown in Table 13-1. Tracking mode is selected automatically when VDD drops below the safe operating voltage of the core.

**Note:** IVR is disabled in Tracking mode, but will consume power. See Section 24.0 “Electrical Specifications” for more information.

<table>
<thead>
<tr>
<th>TABLE 13-1:  IVR POWER MODES - REGULATED</th>
</tr>
</thead>
<tbody>
<tr>
<td>VREGPM1 Bit</td>
</tr>
<tr>
<td>--------------</td>
</tr>
<tr>
<td>x</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>0</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Forced to Low-Power mode by any of the following conditions:

- BOR is enabled
- HFINTOSC is an active peripheral source
- Self-write is active
- ADC is in an active conversion
REGISTER 13-1: VREGCON: VOLTAGE REGULATOR CONTROL REGISTER

<table>
<thead>
<tr>
<th>bit 7-2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unimplemented: Read as ‘0’.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VREGPM1: Voltage Regulator Power Mode Selection bit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 = Power-Save Sleep mode enabled in Sleep. Draws lowest current in Sleep, slower wake-up.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 = Low-Power mode enabled in Sleep. Draws higher current in Sleep, faster wake-up.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved: Maintain this bit set.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
14.0 TEMPERATURE INDICATOR MODULE

This family of devices is equipped with a temperature circuit designed to measure the operating temperature of the silicon die. The circuit’s range of operating temperature falls between of -40°C and +85°C. The output is a voltage that is proportional to the device temperature. The output of the temperature indicator is internally connected to the device ADC.

The circuit may be used as a temperature threshold detector or a more accurate temperature indicator, depending on the level of calibration performed. A one-point calibration allows the circuit to indicate a temperature closely surrounding that point. A two-point calibration allows the circuit to sense the entire range of temperature more accurately. Reference Application Note AN1333, “Use and Calibration of the Internal Temperature Indicator” (DS01333) for more details regarding the calibration process.

14.1 Circuit Operation

Figure 14-1 shows a simplified block diagram of the temperature circuit. The proportional voltage output is achieved by measuring the forward voltage drop across multiple silicon junctions.

Equation 14-1 describes the output characteristics of the temperature indicator.

EQUATION 14-1: \( V_{OUT} \) RANGES

- High Range: \( V_{OUT} = VDD - 4VT \)
- Low Range: \( V_{OUT} = VDD - 2VT \)

The temperature sense circuit is integrated with the Fixed Voltage Reference (FVR) module. See Section 12.0 “Fixed Voltage Reference (FVR)” for more information.

The circuit is enabled by setting the TSEN bit of the FVRCON register. When disabled, the circuit draws no current.

The circuit operates in either high or low range. The high range, selected by setting the TSRNG bit of the FVRCON register, provides a wider output voltage. This provides more resolution over the temperature range, but may be less consistent from part to part. This range requires a higher bias voltage to operate and thus, a higher VDD is needed.

The low range is selected by clearing the TSRNG bit of the FVRCON0 register. The low range generates a lower voltage drop and thus, a lower bias voltage is needed to operate the circuit. The low range is provided for low voltage operation.

14.2 Minimum Operating VDD vs. Minimum Sensing Temperature

When the temperature circuit is operated in low range, the device may be operated at any operating voltage that is within specifications.

When the temperature circuit is operated in high range, the device operating voltage, VDD, must be high enough to ensure that the temperature circuit is correctly biased.

Table 14-1 shows the recommended minimum VDD vs. range setting.

TABLE 14-1: RECOMMENDED VDD VS. RANGE

<table>
<thead>
<tr>
<th>Min. VDD, TSRNG = 1</th>
<th>Min. VDD, TSRNG = 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.6V</td>
<td>1.8V</td>
</tr>
</tbody>
</table>

14.3 Temperature Output

The output of the circuit is measured using the internal Analog-to-Digital Converter. A channel is reserved for the temperature circuit output. Refer to Section 15.0 “Analog-to-Digital Converter (ADC) Module” for detailed information.

14.4 ADC Acquisition Time

To ensure accurate temperature measurements, the user must wait at least 200 \( \mu s \) after the ADC input multiplexer is connected to the temperature indicator output before the conversion is performed. In addition, the user must wait 200 \( \mu s \) between sequential conversions of the temperature indicator output.
### TABLE 14-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE TEMPERATURE INDICATOR

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>FVRCON</td>
<td>FVREN</td>
<td>FVRRDY</td>
<td>TSEN</td>
<td>TSRNG</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ADFVR&lt;1:0&gt;</td>
<td>78</td>
</tr>
<tr>
<td>ADCON</td>
<td>ADCS&lt;2:0&gt;</td>
<td>CHS&lt;2:0&gt;</td>
<td>GO/DONE</td>
<td>ADON</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>88</td>
</tr>
<tr>
<td>ADRES</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>A/D Result Register</td>
<td></td>
<td></td>
<td></td>
<td>89</td>
</tr>
</tbody>
</table>

**Legend:** — = unimplemented location, read as ’0’. Shaded cells are not used by the temperature indicator module.
15.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE

The Analog-to-Digital Converter (ADC) converts an analog input signal to an 8-bit binary representation of that signal. This device uses three analog input channels, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates an 8-bit binary result via successive approximation and stores the conversion result into the ADC result register (ADRES). Figure 15-1 shows the block diagram of the ADC.

The ADC voltage reference is software selectable to be internally generated.

The ADC can generate an interrupt upon completion of a conversion. This interrupt can be used to wake-up the device from Sleep.

**FIGURE 15-1: ADC SIMPLIFIED BLOCK DIAGRAM**

![Block Diagram of the ADC](image)

**Note 1:** When ADON = 0, all multiplexer inputs are disconnected.

**Note 2:** See ADCON register (Register 15-1) for detailed analog channel selection per device.
15.1 ADC Configuration

When configuring and using the ADC the following functions must be considered:

- Port configuration
- Channel selection
- ADC conversion clock source
- Interrupt control

15.1.1 PORT CONFIGURATION

The ADC can be used to convert both analog and digital signals. When converting analog signals, the I/O pin should be configured for analog by setting the associated TRIS and ANSEL bits. Refer to Section 10.0 “I/O Port” for more information.

15.1.2 CHANNEL SELECTION

There are up to five channel selections available:

- AN<2:0> pins
- Temperature Indicator
- FVR (Fixed Voltage Reference) Output

Refer to Section 12.0 “Fixed Voltage Reference (FVR)” and Section 14.0 “Temperature Indicator Module” for more information on these channel selections.

The CHS bits of the ADCON register determine which channel is connected to the sample and hold circuit.

When changing channels, a delay is required before starting the next conversion. Refer to Section 15.2 “ADC Operation” for more information.

15.1.3 ADC VOLTAGE REFERENCE

There is no external voltage reference connections to the ADC. Only VDD can be used as a reference source. The FVR is only available as an input channel and not a VREF+ input to the ADC.

15.1.4 CONVERSION CLOCK

The source of the conversion clock is software selectable via the ADCS bits of the ADCON register (Register 15-1). There are seven possible clock options:

- Fosc/2
- Fosc/4
- Fosc/8
- Fosc/16
- Fosc/32
- Fosc/64
- FRC (dedicated internal RC oscillator)

The time to complete one bit conversion is defined as TAD. One full 8-bit conversion requires 9.5 TAD periods as shown in Figure 15-2.

For correct conversion, the appropriate TAD specification must be met. Refer to the A/D conversion requirements in Section 24.0 “Electrical Specifications” for more information. Table 15-1 gives examples of appropriate ADC clock selections.

**Note:** Unless using the FRC, any changes in the system clock frequency will change the ADC clock frequency, which may adversely affect the ADC result.

**Note:** Analog voltages on any pin that is defined as a digital input may cause the input buffer to conduct excess current.
### TABLE 15-1: ADC CLOCK PERIOD (TAD) VS. DEVICE OPERATING FREQUENCIES

<table>
<thead>
<tr>
<th>ADC Clock Period (Tad)</th>
<th>Device Frequency (Fosc)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC Clock Source</td>
<td>16 MHz</td>
</tr>
<tr>
<td>FOSC/2</td>
<td>000</td>
</tr>
<tr>
<td>FOSC/4</td>
<td>100</td>
</tr>
<tr>
<td>FOSC/8</td>
<td>001</td>
</tr>
<tr>
<td>FOSC/16</td>
<td>101</td>
</tr>
<tr>
<td>FOSC/32</td>
<td>010</td>
</tr>
<tr>
<td>FOSC/64</td>
<td>110</td>
</tr>
<tr>
<td>FRC</td>
<td>x11</td>
</tr>
</tbody>
</table>

**Legend:**
- Shaded cells are outside of recommended range.

**Note**
1. These values violate the minimum required Tad time.
2. For faster conversion times, the selection of another clock source is recommended.
3. The ADC clock period (Tad) and total ADC conversion time can be minimized when the ADC clock is derived from the system clock Fosc. However, the FRC clock source must be used when conversions are to be performed with the device in Sleep mode.

### FIGURE 15-2: ANALOG-TO-DIGITAL CONVERSION TAD CYCLES

- Conversion starts
- Holding capacitor is disconnected from analog input (typically 100 ns)
- Set GO bit
- On the following cycle: ADRES is loaded, GO bit is cleared, ADIF bit is set, holding capacitor is connected to analog input.
15.1.5  INTERRUPTS
The ADC module allows for the ability to generate an interrupt upon completion of an Analog-to-Digital conversion. The ADC Interrupt Flag is the ADIF bit in the PIR1 register. The ADC Interrupt Enable is the ADIE bit in the PIE1 register. The ADIF bit must be cleared in software.

Note: The ADIF bit is set at the completion of every conversion, regardless of whether or not the ADC interrupt is enabled.

This interrupt can be generated while the device is operating or while in Sleep. If the device is in Sleep, the interrupt will wake-up the device. Upon waking from Sleep, the next instruction following the SLEEP instruction is always executed. If the user is attempting to wake-up from Sleep and resume in-line code execution, the GIE and PEIE bits of the INTCON register must be disabled. If the GIE and PEIE bits of the INTCON register are enabled, execution will switch to the Interrupt Service Routine.

15.2  ADC Operation

15.2.1  STARTING A CONVERSION
To enable the ADC module, the ADON bit of the ADCON register must be set to a ‘1’. Setting the GO/DONE bit of the ADCON register to a ‘1’ will start the Analog-to-Digital conversion.

Note: The GO/DONE bit should not be set in the same instruction that turns on the ADC. Refer to Section 15.2.5 “A/D Conversion Procedure”.

15.2.2  COMPLETION OF A CONVERSION
When the conversion is complete, the ADC module will:
• Clear the GO/DONE bit
• Set the ADIF Interrupt Flag bit
• Update the ADRES register with new conversion result

15.2.3  TERMINATING A CONVERSION
If a conversion must be terminated before completion, the GO/DONE bit can be cleared in software. The ADRES register will be updated with the partially complete Analog-to-Digital conversion sample. Incomplete bits will match the last bit converted.

Note: A device Reset forces all registers to their Reset state. Thus, the ADC module is turned off and any pending conversion is terminated.

15.2.4  ADC OPERATION DURING SLEEP
The ADC module can operate during Sleep. This requires the ADC clock source to be set to the FRC option. When the FRC clock source is selected, the ADC waits one additional instruction before starting the conversion. This allows the SLEEP instruction to be executed, which can reduce system noise during the conversion. If the ADC interrupt is enabled, the device will wake-up from Sleep when the conversion completes. If the ADC interrupt is disabled, the ADC module is turned off after the conversion completes, although the ADON bit remains set.

When the ADC clock source is something other than FRC, a SLEEP instruction causes the present conversion to be aborted and the ADC module is turned off, although the ADON bit remains set.
15.2.5  A/D CONVERSION PROCEDURE

This is an example procedure for using the ADC to perform an Analog-to-Digital conversion:

1. Configure Port:
   • Disable pin output driver (Refer to the TRIS register)
   • Configure pin as analog (Refer to the ANSEL register)
   • Disable weak pull-ups either globally (Refer to the OPTION_REG register) or individually (Refer to the appropriate WPUX register)

2. Configure the ADC module:
   • Select ADC conversion clock
   • Select ADC input channel
   • Turn on ADC module

3. Configure ADC interrupt (optional):
   • Clear ADC interrupt flag
   • Enable ADC interrupt
   • Enable peripheral interrupt
   • Enable global interrupt(1)

4. Wait the required acquisition time(2).

5. Start conversion by setting the GO/DONE bit.

6. Wait for ADC conversion to complete by one of the following:
   • Polling the GO/DONE bit
   • Waiting for the ADC interrupt (interrupts enabled)

7. Read ADC Result.

8. Clear the ADC interrupt flag (required if interrupt is enabled).

**Note 1:** The global interrupt can be disabled if the user is attempting to wake-up from Sleep and resume in-line code execution.

**2:** Refer to Section 15.4 “A/D Acquisition Requirements”
15.3 ADC Register Definitions

The following registers are used to control the operation of the ADC.

REGISTER 15-1: ADCON: A/D CONTROL REGISTER 0

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ADCS&lt;2:0&gt;</td>
<td>CHS&lt;2:0&gt;</td>
<td>GO/DONE</td>
<td>ADON</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
u = Bit is unchanged  x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets

bit 7-5  ADCS<2:0>: A/D Conversion Clock Select bits
111 = FRC
110 = Fosc/64
101 = Fosc/16
100 = Fosc/4
011 = FRC
010 = Fosc/32
001 = Fosc/8
000 = Fosc/2

bit 4-2  CHS<2:0>: Analog Channel Select bits
111 = FVR (Fixed Voltage Reference) Buffer Output(2)
110 = Temperature Indicator(1)
101 = Reserved. No channel connected.
100 = Reserved. No channel connected.
011 = Reserved. No channel connected.
010 = AN2
001 = AN1
000 = AN0

bit 1  GO/DONE: A/D Conversion Status bit
If ADON = 1:
1 = A/D conversion in progress (Setting this bit starts the A/D conversion)
0 = A/D conversion not in progress (This bit is automatically cleared by hardware when the A/D conversion is complete.)

If this bit is cleared while a conversion is in progress, the conversion will stop and the results of the conversion up to this point will be transferred to the result registers, but the ADIF interrupt flag bit will not be set.
If ADON = 0:
0 = A/D conversion not in progress

bit 0  ADON: ADC Enable bit
1 = ADC is enabled
0 = ADC is disabled and consumes no operating current

Note 1: See Section 14.0 “Temperature Indicator Module” for more information.
2: See Section 12.0 “Fixed Voltage Reference (FVR)” for more information.
REGISTER 15-2:  ADRES: ADC RESULT REGISTER

<table>
<thead>
<tr>
<th>bit 7-0</th>
<th>ADRES&lt;7:0&gt;: ADC Result Register bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7-0</td>
<td>8-bit result</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- `-n/n` = Value at POR and BOR/Value at all other Resets
15.4 A/D Acquisition Requirements

For the ADC to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 15-3. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD), refer to Figure 15-3. The maximum recommended impedance for analog sources is 10 kΩ. As the source impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed), an A/D acquisition must be done before the conversion can be started. To calculate the minimum acquisition time, Equation 15-1 may be used. This equation assumes that 1/2 LSB error is used (511 steps for the ADC). The 1/2 LSB error is the maximum error allowed for the ADC to meet its specified resolution.

**EQUATION 15-1: ACQUISITION TIME EXAMPLE**

Assumptions: Temperature = 50°C and external impedance of 10kΩ 5.0V VDD

\[
T_{ACQ} = \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient} \\
= T_{AMP} + T_{C} + T_{COFF} \\
= 2\mu s + T_{C} + [(\text{Temperature - 25°C})(0.05\mu s/^\circ C)]
\]

The value for \(T_C\) can be approximated with the following equations:

\[
V_{APPLIED}\left(1 - \frac{1}{2^n + 1}\right) = V_{CHOLD} \quad ;[1] \text{ VCHOLD charged to within 1/2 lsb}
\]

\[
V_{APPLIED}\left(1 - e^{-\frac{T_{C}}{RC}}\right) = V_{CHOLD} \quad ;[2] \text{ VCHOLD charge response to VAPPLIED}
\]

\[
V_{APPLIED}\left(1 - e^{-\frac{T_{C}}{RC}}\right) = V_{APPLIED}\left(1 - \frac{1}{2^n + 1}\right) \quad ;\text{combining } [1] \text{ and } [2]
\]

Note: Where \(n\) = number of bits of the ADC.

**Solving for \(T_C\):**

\[
T_{C} = -CHOLD(R_{IC} + RSS + RS) \ln(1/511) \\
= -10pF(1k\Omega + 7k\Omega + 10k\Omega) \ln(0.001957) \\
= 1.12\mu s
\]

Therefore:

\[
T_{ACQ} = 2\mu s + 1.12\mu s + [(50^\circ C - 25^\circ C)(0.05\mu s/^\circ C)] \\
= 4.37\mu s
\]

**Note 1:** The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

**Note 2:** The charge holding capacitor (CHOLD) is not discharged after each conversion.

**Note 3:** The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.
FIGURE 15-3: ANALOG INPUT MODEL

Legend:
- CHOLD = Sample/Hold Capacitance
- CPIN = Input Capacitance
- ILEAKAGE = Leakage current at the pin due to various junctions
- RIC = Interconnect Resistance
- RSS = Resistance of Sampling Switch
- SS = Sampling Switch
- VT = Threshold Voltage

Note 1: Refer to Section 24.0 “Electrical Specifications”.

FIGURE 15-4: ADC TRANSFER FUNCTION

Legend:
- FS = Full-Scale
- VREF = Reference Voltage
- 0.5 LSB = Half a least significant bit
- 1.5 LSB = One and a half least significant bits

Note 1: Refer to Section 24.0 “Electrical Specifications”.
### TABLE 15-2: SUMMARY OF REGISTERS ASSOCIATED WITH ADC

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADCON</td>
<td>ADCS&lt;2:0&gt;</td>
<td>CHS&lt;2:0&gt;</td>
<td>GO/DONE</td>
<td>ADON</td>
<td>88</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADRES</td>
<td>ADRES&lt;7:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ANSA2</td>
<td>ANSA1</td>
<td>ANSA0</td>
</tr>
<tr>
<td>ANSELA</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>FVRCON</td>
<td>FVREN</td>
<td>FVRRDY</td>
<td>TSEN</td>
<td>TSRNG</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ADFVR&lt;1:0&gt;</td>
<td>78</td>
</tr>
<tr>
<td>INTCION</td>
<td>GIE</td>
<td>PEIE</td>
<td>TMR0IE</td>
<td>INTE</td>
<td>IOCIE</td>
<td>TMR0IF</td>
<td>INTF</td>
<td>IOCIF</td>
<td>40</td>
</tr>
<tr>
<td>PIE1</td>
<td>—</td>
<td>ADIE</td>
<td>—</td>
<td>NCO1E</td>
<td>CLC1E</td>
<td>—</td>
<td>TMR2IE</td>
<td>—</td>
<td>41</td>
</tr>
<tr>
<td>PIR1</td>
<td>—</td>
<td>ADIF</td>
<td>—</td>
<td>NCO1F</td>
<td>CLC1F</td>
<td>—</td>
<td>TMR2IF</td>
<td>—</td>
<td>42</td>
</tr>
<tr>
<td>TRISA</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TRISA2</td>
<td>TRISA1</td>
<td>TRISA0</td>
</tr>
</tbody>
</table>

**Legend:**  
\( \times \) = unknown, \( \_ \) = unchanged, \( — \) = unimplemented read as '0', \( q \) = value depends on condition. Shaded cells are not used for ADC module.
16.0 TIMER0 MODULE

The Timer0 module is an 8-bit timer/counter with the following features:
- 8-bit timer/counter register (TMR0)
- 8-bit prescaler (independent of Watchdog Timer)
- Programmable internal or external clock source
- Programmable external clock edge selection
- Interrupt on overflow

Figure 16-1 is a block diagram of the Timer0 module.

16.1 Timer0 Operation

The Timer0 module can be used as either an 8-bit timer or an 8-bit counter.

16.1.1 8-BIT TIMER MODE

The Timer0 module will increment every instruction cycle, if used without a prescaler. 8-Bit Timer mode is selected by clearing the T0CS bit of the OPTION_REG register.

When TMR0 is written, the increment is inhibited for two instruction cycles immediately following the write.

Note: The value written to the TMR0 register can be adjusted, in order to account for the two instruction cycle delay when TMR0 is written.

16.1.2 8-BIT COUNTER MODE

In 8-Bit Counter mode, the Timer0 module will increment on every rising or falling edge of the T0CKI pin.

8-Bit Counter mode using the T0CKI pin is selected by setting the T0CS bit in the OPTION_REG register to '1'.

The rising or falling transition of the incrementing edge for the external input source is determined by the T0SE bit in the OPTION_REG register.
16.1.3 SOFTWARE PROGRAMMABLE PRESCALER

A single software programmable prescaler is available for use with Timer0. The prescaler assignment is controlled by the PSA bit of the OPTION_REG register. To assign the prescaler to Timer0, the PSA bit must be cleared to a '0'.

There are eight prescaler options for the Timer0 module ranging from 1:2 to 1:256. The prescale values are selectable via the PS<2:0> bits of the OPTION_REG register.

The prescaler is not readable or writable. When assigned to the Timer0 module, all instructions writing to the TMR0 register will clear the prescaler.

16.1.4 TIMER0 INTERRUPT

Timer0 will generate an interrupt when the TMR0 register overflows from FFh to 00h. The TMR0IF interrupt flag bit of the INTCON register is set every time the TMR0 register overflows, regardless of whether or not the Timer0 interrupt is enabled. The TMR0IF bit can only be cleared in software. The Timer0 interrupt enable is the TMR0IE bit of the INTCON register.

Note: The Timer0 interrupt cannot wake the processor from Sleep since the timer is frozen during Sleep.

16.1.5 8-BIT COUNTER MODE SYNCHRONIZATION

When in 8-Bit Counter mode, the incrementing edge on the T0CKI pin must be synchronized to the instruction clock. Synchronization can be accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the instruction clock. The high and low periods of the external clocking source must meet the timing requirements as shown in Section 24.0 “Electrical Specifications”.
REGISTER 16-1: OPTION_REG: OPTION REGISTER

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>WPUEN(1)</td>
<td>INTEDG</td>
<td>T0CS</td>
<td>T0SE</td>
<td>PSA</td>
<td>PS&lt;2:0&gt;</td>
<td></td>
<td></td>
<td>95</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

**bit 7 WPUEN:** Weak Pull-up Enable bit(1)
- 1 = Weak pull-ups are disabled
- 0 = Weak pull-ups are enabled by individual PORT latch values

**bit 6 INTEDG:** Interrupt Edge Select bit
- 1 = Interrupt on rising edge of INT pin
- 0 = Interrupt on falling edge of INT pin

**bit 5 T0CS:** TMR0 Clock Source Select bit
- 1 = Transition on T0CKI pin
- 0 = Internal instruction cycle clock (Fosc/4)

**bit 4 T0SE:** TMR0 Source Edge Select bit
- 1 = Increment on high-to-low transition on T0CKI pin
- 0 = Increment on low-to-high transition on T0CKI pin

**bit 3 PSA:** Prescaler Assignment bit
- 1 = Prescaler is inactive and has no effect on the Timer 0 module
- 0 = Prescaler is assigned to the Timer0 module

**bit 2-0 PS<2:0>:** Prescaler Rate Select bits

<table>
<thead>
<tr>
<th>Bit Value</th>
<th>TMR0 Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>1 : 2</td>
</tr>
<tr>
<td>001</td>
<td>1 : 4</td>
</tr>
<tr>
<td>010</td>
<td>1 : 8</td>
</tr>
<tr>
<td>011</td>
<td>1 : 16</td>
</tr>
<tr>
<td>100</td>
<td>1 : 32</td>
</tr>
<tr>
<td>101</td>
<td>1 : 64</td>
</tr>
<tr>
<td>110</td>
<td>1 : 128</td>
</tr>
<tr>
<td>111</td>
<td>1 : 256</td>
</tr>
</tbody>
</table>

**Note 1:** WPUEN does not disable the pull-up for the MCLR input when MCLR = 1.

TABLE 16-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER0

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>TMR0IE</td>
<td>INTE</td>
<td>IOCIE</td>
<td>TMR0IF</td>
<td>INTF</td>
<td>IOCIF</td>
<td>40</td>
</tr>
<tr>
<td>OPTION_REG</td>
<td>WPUEN</td>
<td>INTEDG</td>
<td>T0CS</td>
<td>T0SE</td>
<td>PSA</td>
<td>PS&lt;2:0&gt;</td>
<td></td>
<td></td>
<td>95</td>
</tr>
<tr>
<td>TMR0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Timer0 module Register 40</td>
</tr>
<tr>
<td>TRISA</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TRISA2</td>
<td>TRISA1</td>
<td>TRISA0 69</td>
</tr>
</tbody>
</table>

Legend: — = Unimplemented locations, read as ‘0’, u = unchanged, x = unknown. Shaded cells are not used by the Timer0 module.
17.0 TIMER2 MODULE

The Timer2 module is an 8-bit timer with the following features:

- 8-bit timer register (TMR2)
- 8-bit period register (PR2)
- Interrupt on TMR2 match with PR2
- Software programmable prescaler (1:1, 1:4, 1:16, 1:64)
- Software programmable postscaler (1:1 to 1:16)

See Figure 17-1 for a block diagram of Timer2.

17.1 Timer2 Operation

The clock input to the Timer2 module is the system instruction clock (Fosc/4). The clock is fed into the Timer2 prescaler, which has prescale options of 1:1, 1:4 or 1:64. The output of the prescaler is then used to increment the TMR2 register.

The values of TMR2 and PR2 are constantly compared to determine when they match. TMR2 will increment from 00h until it matches the value in PR2. When a match occurs, two things happen:

- TMR2 is reset to 00h on the next increment cycle.
- The Timer2 postscaler is incremented.

The match output of the Timer2/PR2 comparator is then fed into the Timer2 postscaler. The postscaler has postscale options of 1:1 to 1:16 inclusive. The output of the Timer2 postscaler is used to set the TMR2IF interrupt flag bit in the PIR1 register.

Note: TMR2 is not cleared when T2CON is written.

FIGURE 17-1: TIMER2 BLOCK DIAGRAM

The TMR2 and PR2 registers are both fully readable and writable. On any Reset, the TMR2 register is set to 00h and the PR2 register is set to FFh.

Timer2 is turned on by setting the TMR2ON bit in the T2CON register to a '1'. Timer2 is turned off by clearing the TMR2ON bit to a '0'.

The Timer2 prescaler is controlled by the T2CKPS bits in the T2CON register. The Timer2 postscaler is controlled by the TOUTPS bits in the T2CON register. The prescaler and postscaler counters are cleared when:

- A write to TMR2 occurs.
- A write to T2CON occurs.
- Any device Reset occurs (Power-on Reset, MCLR Reset, Watchdog Timer Reset, or Brown-out Reset).
REGISTER 17-1: T2CON: TIMER2 CONTROL REGISTER

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6-3</th>
<th>Bit 2</th>
<th>Bit 1-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>TOUTPS&lt;3:0&gt;</td>
<td>TMR2ON</td>
<td>T2CKPS&lt;1:0&gt;</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared

bit 7  Unimplemented: Read as '0'
bit 6-3  TOUTPS<3:0>: Timer2 Output Postscaler Select bits
1 1111  = 1:16 Postscaler
1 1110  = 1:15 Postscaler
1 1101  = 1:14 Postscaler
1 1100  = 1:13 Postscaler
1 1011  = 1:12 Postscaler
1 1010  = 1:11 Postscaler
1 1001  = 1:10 Postscaler
1 1000  = 1:9 Postscaler
0 1111  = 1:8 Postscaler
0 1110  = 1:7 Postscaler
0 1101  = 1:6 Postscaler
0 1100  = 1:5 Postscaler
0 1011  = 1:4 Postscaler
0 1010  = 1:3 Postscaler
0 1001  = 1:2 Postscaler
0 1000  = 1:1 Postscaler
bit 2  TMR2ON: Timer2 On bit
1 = Timer2 is on
0 = Timer2 is off
bit 1-0  T2CKPS<1:0>: Timer2 Clock Prescale Select bits
1 11 = Prescaler is 64
1 10 = Prescaler is 16
0 11 = Prescaler is 4
0 10 = Prescaler is 1
0 01 = Prescaler is 2
0 00 = Prescaler is 1

TABLE 17-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER2

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>TMR0IE</td>
<td>INTE</td>
<td>IOCE</td>
<td>TMR0IF</td>
<td>INTF</td>
<td>IOCF</td>
<td>40</td>
</tr>
<tr>
<td>PIE1</td>
<td>—</td>
<td>ADIE</td>
<td>—</td>
<td>NCO1IE</td>
<td>CLC1IE</td>
<td>—</td>
<td>TMR2IE</td>
<td>—</td>
<td>41</td>
</tr>
<tr>
<td>PIR1</td>
<td>—</td>
<td>ADIF</td>
<td>—</td>
<td>NCO1IF</td>
<td>CLC1IF</td>
<td>—</td>
<td>TMR2IF</td>
<td>—</td>
<td>42</td>
</tr>
</tbody>
</table>

PR2  Timer2 module Period Register  96
TMR2  Timer2 module Register  96
T2CON  —  TOUTPS<3:0>  TMR2ON  T2CKPS<1:0>  97

Legend:  x = unknown,  u = unchanged,  -n/n = unimplemented read as '0'. Shaded cells are not used for Timer2 module.
18.0 PULSE-WIDTH MODULATION (PWM) MODULE

The PWM module generates a Pulse-Width Modulated signal determined by the duty cycle, period, and resolution that are configured by the following registers:
- PR2
- T2CON
- PWMxDCH
- PWMxDCL
- PWMxCON

Figure 18-1 shows a simplified block diagram of PWM operation. Figure 18-2 shows a typical waveform of the PWM signal.

For a step-by-step procedure on how to set up this module for PWM operation, refer to Section 18.1.9 “Setup for PWM Operation using PWMx Pins”.

Note 1: 8-bit timer is concatenated with the two Least Significant bits of 1/Fosc adjusted by the Timer2 prescaler to create a 10-bit time base.
18.1 PWMx Pin Configuration

All PWM outputs are multiplexed with the PORT data latch. The user must configure the pins as outputs by clearing the associated TRIS bits.

Note: Clearing the PWMxOE bit will relinquish control of the PWMx pin.

18.1.1 FUNDAMENTAL OPERATION

The PWM module produces a 10-bit resolution output. Timer2 and PR2 set the period of the PWM. The PWMxDCL and PWMxDCH registers configure the duty cycle. The period is common to all PWM modules, whereas the duty cycle is independently controlled.

Note: The Timer2 postscaler is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

All PWM outputs associated with Timer2 are set when TMR2 is cleared. Each PWMx is cleared when TMR2 is equal to the value specified in the corresponding PWMxDCH (8 MSb) and PWMxDCL<7:6> (2 LSb) registers. When the value is greater than or equal to PR2, the PWM output is never cleared (100% duty cycle).

Note: The PWMxDCH and PWMxDCL registers are double buffered. The buffers are updated when Timer2 matches PR2. Care should be taken to update both registers before the timer match occurs.

18.1.2 PWM OUTPUT POLARITY

The output polarity is inverted by setting the PWMxPOL bit of the PWMxCON register.

18.1.3 PWM PERIOD

The PWM period is specified by the PR2 register of Timer2. The PWM period can be calculated using the formula of Equation 18-1.

EQUATION 18-1: PWM PERIOD

\[
PWM \text{ Period} = \frac{[(PR2) + 1] \cdot 4 \cdot T_{osc}}{(TMR2 \text{ Prescale Value})}
\]

Note: \( T_{osc} = 1/F_{osc} \)

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The PWM output is active. (Exception: When the PWM duty cycle = 0%, the PWM output will remain inactive.)
- The PWMxDCH and PWMxDCL register values are latched into the buffers.

Note: The Timer2 postscaler has no effect on the PWM operation.

18.1.4 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to the PWMxDCH and PWMxDCL register pair. The PWMxDCH register contains the eight MSbs and the PWMxDCL<7:6>, the two LSbs. The PWMxDCH and PWMxDCL registers can be written to at any time.

Equation 18-2 is used to calculate the PWM pulse width.

Equation 18-3 is used to calculate the PWM duty cycle ratio.

EQUATION 18-2: PULSE WIDTH

\[
Pulse \text{ Width} = (PWMxDCH;PWMxDCL<7:6>) \cdot \frac{T_{osc}}{(TMR2 \text{ Prescale Value})}
\]

Note: \( T_{osc} = 1/F_{osc} \)

EQUATION 18-3: DUTY CYCLE RATIO

\[
Duty \text{ Cycle Ratio} = \frac{(PWMxDCH;PWMxDCL<7:6>)}{4(\text{PR2} + 1)}
\]

The 8-bit timer TMR2 register is concatenated with the two Least Significant bits of 1/Fosc, adjusted by the Timer2 prescaler to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.
18.1.5 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is ten bits when PR2 is 255. The resolution is a function of the PR2 register value as shown by Equation 18-4.

**EQUATION 18-4: PWM RESOLUTION**

\[
\text{Resolution} = \frac{\log[4(\text{PR2} + 1)]}{\log(2)} \quad \text{bits}
\]

Note: If the pulse-width value is greater than the period the assigned PWM pin(s) will remain unchanged.

**TABLE 18-1: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 20 MHz)**

<table>
<thead>
<tr>
<th>PWM Frequency</th>
<th>0.31 kHz</th>
<th>4.88 kHz</th>
<th>19.53 kHz</th>
<th>78.12 kHz</th>
<th>156.3 kHz</th>
<th>208.3 kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer Prescale (1, 4, 64)</td>
<td>64</td>
<td>4</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>PR2 Value</td>
<td>0xFF</td>
<td>0xFF</td>
<td>0xFF</td>
<td>0x3F</td>
<td>0x1F</td>
<td>0x17</td>
</tr>
<tr>
<td>Maximum Resolution (bits)</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>8</td>
<td>7</td>
<td>6.6</td>
</tr>
</tbody>
</table>

**TABLE 18-2: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 8 MHz)**

<table>
<thead>
<tr>
<th>PWM Frequency</th>
<th>0.31 kHz</th>
<th>4.90 kHz</th>
<th>19.61 kHz</th>
<th>76.92 kHz</th>
<th>153.85 kHz</th>
<th>200.0 kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer Prescale (1, 4, 64)</td>
<td>64</td>
<td>4</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>PR2 Value</td>
<td>0x65</td>
<td>0x65</td>
<td>0x65</td>
<td>0x19</td>
<td>0x0C</td>
<td>0x09</td>
</tr>
<tr>
<td>Maximum Resolution (bits)</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>6</td>
<td>5</td>
<td>5</td>
</tr>
</tbody>
</table>

18.1.6 OPERATION IN SLEEP MODE

In Sleep mode, the TMR2 register will not increment and the state of the module will not change. If the PWMx pin is driving a value, it will continue to drive that value. When the device wakes up, TMR2 will continue from its previous state.

18.1.7 CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency (Fosc). Any changes in the system clock frequency will result in changes to the PWM frequency. Refer to Section 4.0 “Oscillator Module” for additional details.

18.1.8 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the PWM registers to their Reset states.
18.1.9 SETUP FOR PWM OPERATION USING PWMx PINS

The following steps should be taken when configuring the module for PWM operation using the PWMx pins:

1. Disable the PWMx pin output driver(s) by setting the associated TRIS bit(s).
2. Clear the PWMxCON register.
3. Load the PR2 register with the PWM period value.
4. Clear the PWMxDCH register and bits <7:6> of the PWMxDCL register.
5. Configure and start Timer2:
   • Clear the TMR2IF interrupt flag bit of the PIR1 register. See Note below.
   • Configure the T2CKPS bits of the T2CON register with the Timer2 prescale value.
   • Enable Timer2 by setting the TMR2ON bit of the T2CON register.
6. Enable PWM output pin and wait until Timer2 overflows, TMR2IF bit of the PIR1 register is set. See Note below.
7. Enable the PWMx pin output driver(s) by clearing the associated TRIS bit(s) and setting the PWMxOE bit of the PWMxCON register.
8. Configure the PWM module by loading the PWMxCON register with the appropriate values.

**Note 1:** In order to send a complete duty cycle and period on the first PWM output, the above steps must be followed in the order given. If it is not critical to start with a complete PWM signal, then move Step 8 to replace Step 4.

**Note 2:** For operation with other peripherals only, disable PWMx pin outputs.
### 18.2 PWM Register Definitions

#### REGISTER 18-1: PWMxCON: PWM CONTROL REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>PWMxEN: PWM Module Enable bit</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>PWMxOE: PWM Module Output Enable bit</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>PWMxOUT: PWM Module Output Value bit</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>PWMxPOL: PWMx Output Polarity Select bit</td>
<td></td>
</tr>
</tbody>
</table>

#### Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared

- **PWMxEN**: PWM Module Enable bit
  - **1** = PWM module is enabled
  - **0** = PWM module is disabled

- **PWMxOE**: PWM Module Output Enable bit
  - **1** = Output to PWMx pin is enabled
  - **0** = Output to PWMx pin is disabled

- **PWMxOUT**: PWM Module Output Value bit

- **PWMxPOL**: PWMx Output Polarity Select bit
  - **1** = PWM output is active-low.
  - **0** = PWM output is active-high.

- **Unimplemented**: Read as ‘0’
**REGISTER 18-2: PWMxDCH: PWM DUTY CYCLE HIGH BITS**

<table>
<thead>
<tr>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared

bit 7-0 **PWMxDCH<7:0>: PWM Duty Cycle Most Significant bits**
These bits are the MSbs of the PWM duty cycle. The two LSbs are found in the PWMxDCL Register.

**REGISTER 18-3: PWMxDCL: PWM DUTY CYCLE LOW BITS**

<table>
<thead>
<tr>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared

bit 7-6 **PWMxDCL<7:6>: PWM Duty Cycle Least Significant bits**
These bits are the LSbs of the PWM duty cycle. The MSbs are found in the PWMxDCH Register.

bit 5-0 **Unimplemented**: Read as ‘0’

**TABLE 18-3: SUMMARY OF REGISTERS ASSOCIATED WITH PWM**

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANSELA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ANSA2</td>
<td>ANSA1</td>
<td>ANSA0</td>
<td>70</td>
</tr>
<tr>
<td>LATA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LATA2</td>
<td>LATA1</td>
<td>LATA0</td>
<td>70</td>
</tr>
<tr>
<td>PORTA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RA3</td>
<td>RA2</td>
<td>RA1</td>
<td>RA0</td>
</tr>
<tr>
<td>PR2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Timer2 module Period Register</td>
</tr>
<tr>
<td>PWM1CON</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PWM1CON&lt;102&gt;</td>
</tr>
<tr>
<td>PWM1DCH</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PWM1DCH&lt;103&gt;</td>
</tr>
<tr>
<td>PWM1DCL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PWM1DCL&lt;103&gt;</td>
</tr>
<tr>
<td>PWM2CON</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PWM2CON&lt;102&gt;</td>
</tr>
<tr>
<td>PWM2DCH</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PWM2DCH&lt;103&gt;</td>
</tr>
<tr>
<td>PWM2DCL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PWM2DCL&lt;103&gt;</td>
</tr>
<tr>
<td>T2CON</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TOUTPS&lt;3:0&gt;</td>
<td>TMR2ON</td>
<td>T2CKPS&lt;1:0&gt;</td>
</tr>
<tr>
<td>TMR2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Timer2 module Register</td>
</tr>
<tr>
<td>TRISA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TRISA2</td>
<td>TRISA1</td>
</tr>
</tbody>
</table>

**Legend:**
- ‘-’ = Unimplemented locations, read as ‘0’, u = unchanged, x = unknown. Shaded cells are not used by the PWM.
19.0 CONFIGURABLE LOGIC CELL (CLC)

The Configurable Logic Cell (CLCx) provides programmable logic that operates outside the speed limitations of software execution. The logic cell selects any combination of the eight input signals and through the use of configurable gates reduces the selected inputs to four logic lines that drive one of eight selectable single-output logic functions.

Input sources are a combination of the following:

- Two I/O pins
- Internal clocks
- Peripherals
- Register bits

The output can be directed internally to peripherals and to an output pin.

FIGURE 19-1: CLCx SIMPLIFIED BLOCK DIAGRAM

Refer to Figure 19-1 for a simplified diagram showing signal flow through the CLCx.

Possible configurations include:

- Combinatorial Logic
  - AND
  - NAND
  - AND-OR
  - AND-OR-INVERT
  - OR-XOR
  - OR-XNOR
- Latches
  - S-R
  - Clocked D with Set and Reset
  - Transparent D with Set and Reset
  - Clocked J-K with Reset
19.1 CLCx Setup

Programming the CLCx module is performed by configuring the four stages in the logic signal flow. The four stages are:

- Data selection
- Data gating
- Logic function selection
- Output polarity

Each stage is set up at run time by writing to the corresponding CLCx Special Function Registers. This has the added advantage of permitting logic reconfiguration on-the-fly during program execution.

19.1.1 DATA SELECTION

There are eight signals available as inputs to the configurable logic. Four 8-input multiplexers are used to select the inputs to pass on to the next stage.

Data inputs are selected with the CLCxSEL0 and CLCxSEL1 registers (Register 19-3 and Register 19-4, respectively).

Data selection is through four multiplexers as indicated on the left side of Figure 19-2. Data inputs in the figure are identified by a generic numbered input name.

Table 19-1 correlates the generic input name to the actual signal for each CLC module. The columns labeled lcxd1 through lcxd4 indicate the MUX output for the selected data input. D1S through D4S are abbreviations for the MUX select input codes: LCxD1S<2:0> through LCxD4S<2:0>, respectively. Selecting a data input in a column excludes all other inputs in that column.

**Note:** Data selections are undefined at power-up.

<table>
<thead>
<tr>
<th>Data Input</th>
<th>lcxd1 D1S</th>
<th>lcxd2 D2S</th>
<th>lcxd3 D3S</th>
<th>lcxd4 D4S</th>
<th>CLC 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLCxIN[0]</td>
<td>000</td>
<td>000</td>
<td>000</td>
<td>000</td>
<td>CLCx</td>
</tr>
<tr>
<td>CLCxIN[1]</td>
<td>001</td>
<td>001</td>
<td>001</td>
<td>001</td>
<td>CLCxIN1</td>
</tr>
<tr>
<td>CLCxIN[2]</td>
<td>010</td>
<td>010</td>
<td>010</td>
<td>010</td>
<td>CLCxIN2</td>
</tr>
<tr>
<td>CLCxIN[3]</td>
<td>011</td>
<td>011</td>
<td>011</td>
<td>011</td>
<td>PWM1</td>
</tr>
<tr>
<td>CLCxIN[4]</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>PWM2</td>
</tr>
<tr>
<td>CLCxIN[5]</td>
<td>101</td>
<td>101</td>
<td>101</td>
<td>101</td>
<td>NCOx</td>
</tr>
<tr>
<td>CLCxIN[6]</td>
<td>110</td>
<td>110</td>
<td>110</td>
<td>110</td>
<td>Fosc</td>
</tr>
<tr>
<td>CLCxIN[7]</td>
<td>111</td>
<td>111</td>
<td>111</td>
<td>111</td>
<td>LFINTOSC</td>
</tr>
</tbody>
</table>

19.1.2 DATA GATING

Outputs from the input multiplexers are directed to the desired logic function input through the data gating stage. Each data gate can direct any combination of the four selected inputs.

**Note:** Data gating is undefined at power-up.

The gate stage is more than just signal direction. The gate can be configured to direct each input signal as inverted or non-inverted data. Directed signals are ANDed together in each gate. The output of each gate can be inverted before going on to the logic function stage.

The gating is in essence a 1-to-4 input AND/NAND/OR/NOR gate. When every input is inverted and the output is inverted, the gate is an OR of all enabled data inputs. When the inputs and output are not inverted, the gate is an AND or all enabled inputs.

Table 19-2 summarizes the basic logic that can be obtained in gate 1 by using the gate logic select bits. The table shows the logic of four input variables, but each gate can be configured to use less than four. If no inputs are selected, the output will be zero or one, depending on the gate output polarity bit.

**TABLE 19-2: DATA GATING LOGIC**

<table>
<thead>
<tr>
<th>CLCxGLS0</th>
<th>LCxGyPOL</th>
<th>Gate Logic</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x55</td>
<td>1</td>
<td>AND</td>
</tr>
<tr>
<td>0x55</td>
<td>0</td>
<td>NAND</td>
</tr>
<tr>
<td>0xAA</td>
<td>1</td>
<td>NOR</td>
</tr>
<tr>
<td>0xAA</td>
<td>0</td>
<td>OR</td>
</tr>
<tr>
<td>0x00</td>
<td>0</td>
<td>Logic 0</td>
</tr>
<tr>
<td>0x00</td>
<td>1</td>
<td>Logic 1</td>
</tr>
</tbody>
</table>

It is possible (but not recommended) to select both the true and negated values of an input. When this is done, the gate output is zero, regardless of the other inputs, but may emit logic glitches (transient-induced pulses). If the output of the channel must be zero or one, the recommended method is to set all gate bits to zero and use the gate polarity bit to set the desired level.

Data gating is configured with the logic gate select registers as follows:

- Gate 1: CLCxGLS0 (Register 19-5)
- Gate 2: CLCxGLS1 (Register 19-6)
- Gate 3: CLCxGLS2 (Register 19-7)
- Gate 4: CLCxGLS3 (Register 19-8)

Register number suffixes are different than the gate numbers because other variations of this module have multiple gate selections in the same register.

Data gating is indicated in the right side of Figure 19-2. Only one gate is shown in detail. The remaining three gates are configured identically with the exception that the data enables correspond to the enables for that gate.
19.1.3 LOGIC FUNCTION

There are eight available logic functions including:
- AND-OR
- OR-XOR
- AND
- S-R Latch
- D Flip-Flop with Set and Reset
- D Flip-Flop with Reset
- J-K Flip-Flop with Reset
- Transparent Latch with Set and Reset

Logic functions are shown in Figure 19-3. Each logic function has four inputs and one output. The four inputs are the four data gate outputs of the previous stage. The output is fed to the inversion stage and from there to other peripherals, an output pin, and back to the CLCx itself.

19.1.4 OUTPUT POLARITY

The last stage in the configurable logic cell is the output polarity. Setting the LCxPOL bit of the CLCxCON register inverts the output signal from the logic stage. Changing the polarity while the interrupts are enabled will cause an interrupt for the resulting output transition.

19.1.5 CLCx SETUP STEPS

The following steps should be followed when setting up the CLCx:

- Disable CLCx by clearing the LCxEN bit.
- Select desired inputs using CLCxSEL0 and CLCxSEL1 registers (See Table 19-1).
- Clear any associated ANSEL bits.
- Set all TRIS bits associated with inputs.
- Clear all TRIS bits associated with outputs.
- Enable the chosen inputs through the four gates using CLCxGLS0, CLCxGLS1, CLCxGLS2, and CLCxGLS3 registers.
- Select the gate output polarities with the LCxPOLy bits of the CLCxPOL register.
- Select the desired logic function with the LCxMODE<2:0> bits of the CLCxCON register.
- Select the desired polarity of the logic output with the LCxPOL bit of the CLCxPOL register. (This step may be combined with the previous gate output polarity step).
- If driving the CLCx pin, set the LCxOE bit of the CLCxCON register and also clear the TRIS bit corresponding to that output.
- If interrupts are desired, configure the following bits:
  - Set the LCxINTP bit in the CLCxCON register for rising event.
  - Set the LCxINTN bit in the CLCxCON register or falling event.
  - Set the CLCxIE bit of the associated PIE registers.
  - Set the GIE and PEIE bits of the INTCON register.
- Enable the CLCx by setting the LCxEN bit of the CLCxCON register.
19.2 CLCx Interrupts

An interrupt will be generated upon a change in the output value of the CLCx when the appropriate interrupt enables are set. A rising edge detector and a falling edge detector are present in each CLC for this purpose. The CLCxIF bit of the associated PIR registers will be set when either edge detector is triggered and its associated enable bit is set. The LCxINTP enables rising edge interrupts and the LCxINTN bit enables falling edge interrupts. Both are located in the CLCxCON register.

To fully enable the interrupt, set the following bits:
- LCxON bit of the CLCxCON register
- CLCxIE bit of the associated PIE registers
- LCxINTP bit of the CLCxCON register (for a rising edge detection)
- LCxINTN bit of the CLCxCON register (for a falling edge detection)
- PEIE and GIE bits of the INTCON register

The CLCxIF bit of the associated PIR registers must be cleared in software as part of the interrupt service. If another edge is detected while this flag is being cleared, the flag will still be set at the end of the sequence.

19.3 Effects of a Reset

The CLCxCON register is cleared to zero as the result of a Reset. All other selection and gating values remain unchanged.

19.4 Operation During Sleep

The selection, gating, and logic functions are not affected by Sleep. Operation will continue provided that the source signals are also not affected by Sleep.
FIGURE 19-2: INPUT DATA SELECTION AND GATING

Note: All controls are undefined at power-up.
FIGURE 19-3: PROGRAMMABLE LOGIC FUNCTIONS

**AND - OR**

<table>
<thead>
<tr>
<th>LCxMODE&lt;2:0&gt;</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>4-Input AND</td>
</tr>
<tr>
<td>010</td>
<td>1-Input D Flip-Flop with S and R</td>
</tr>
<tr>
<td>100</td>
<td>J-K Flip-Flop with R</td>
</tr>
<tr>
<td>110</td>
<td>1-Input Transparent Latch with S and R</td>
</tr>
</tbody>
</table>

**OR - XOR**

<table>
<thead>
<tr>
<th>LCxMODE&lt;2:0&gt;</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>001</td>
<td>S-R Latch</td>
</tr>
<tr>
<td>011</td>
<td>2-Input D Flip-Flop with R</td>
</tr>
<tr>
<td>101</td>
<td>1-Input Transparent Latch with S and R</td>
</tr>
</tbody>
</table>
19.5 CLC Control Registers

REGISTER 19-1: CLCxCON: CONFIGURABLE LOGIC CELL CONTROL REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCxEN</td>
<td>LCxOE</td>
<td>LCxOUT</td>
<td>LCxINTP</td>
<td>LCxINTN</td>
<td>LCxMODE&lt;2:0&gt;</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

bit 7

**LCxEN:** Configurable Logic Cell Enable bit
1 = Configurable Logic Cell is enabled and mixing input signals
0 = Configurable Logic Cell is disabled and has logic zero output

bit 6

**LCxOE:** Configurable Logic Cell Output Enable bit
1 = Configurable Logic Cell port pin output enabled
0 = Configurable Logic Cell port pin output disabled

bit 5

**LCxOUT:** Configurable Logic Cell Data Output bit
Read-only: logic cell output data, after LCxPOL; sampled from lcx_out wire.

bit 4

**LCxINTP:** Configurable Logic Cell Positive Edge Going Interrupt Enable bit
1 = CLCxIF will be set when a rising edge occurs on lcx_out
0 = CLCxIF will not be set

bit 3

**LCxINTN:** Configurable Logic Cell Negative Edge Going Interrupt Enable bit
1 = CLCxIF will be set when a falling edge occurs on lcx_out
0 = CLCxIF will not be set

bit 2-0

**LCxMODE<2:0>:** Configurable Logic Cell Functional Mode bits
111 = Cell is 1-input transparent latch with S and R
110 = Cell is J-K Flip-Flop with R
101 = Cell is 2-input D Flip-Flop with R
100 = Cell is 1-input D Flip-Flop with S and R
011 = Cell is S-R latch
010 = Cell is 4-input AND
001 = Cell is OR-XOR
000 = Cell is AND-OR

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Reset
- '1' = Bit is set
- '0' = Bit is cleared
## REGISTER 19-2: CLCxPOL: SIGNAL POLARITY CONTROL REGISTER

<table>
<thead>
<tr>
<th>bit</th>
<th>LCxPOL</th>
<th>LCxG4POL</th>
<th>LCxG3POL</th>
<th>LCxG2POL</th>
<th>LCxG1POL</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6-4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>LCxG4POL</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>LCxG3POL</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>LCxG2POL</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>LCxG1POL</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Reset
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

### Bit 7

**LCxPOL**: LCOUT Polarity Control bit

- **1** = The output of the logic cell is inverted
- **0** = The output of the logic cell is not inverted

### Bit 6-4

**Unimplemented**: Read as ‘0’

### Bit 3

**LCxG4POL**: Gate 4 Output Polarity Control bit

- **1** = The output of gate 4 is inverted when applied to the logic cell
- **0** = The output of gate 4 is not inverted

### Bit 2

**LCxG3POL**: Gate 3 Output Polarity Control bit

- **1** = The output of gate 3 is inverted when applied to the logic cell
- **0** = The output of gate 3 is not inverted

### Bit 1

**LCxG2POL**: Gate 2 Output Polarity Control bit

- **1** = The output of gate 2 is inverted when applied to the logic cell
- **0** = The output of gate 2 is not inverted

### Bit 0

**LCxG1POL**: Gate 1 Output Polarity Control bit

- **1** = The output of gate 1 is inverted when applied to the logic cell
- **0** = The output of gate 1 is not inverted
## REGISTER 19-3: CLCxSEL0: MULTIPLEXER DATA 1 AND 2 SELECT REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>U-0</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>LCxD2S&lt;2:0&gt;(1)</td>
<td></td>
<td></td>
<td></td>
<td>LCxD1S&lt;2:0&gt;(1)</td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **’1’** = Bit is set
- **’0’** = Bit is cleared

| bit 7 | **Unimplemented**: Read as ‘0’ |
| bit 6-4 | **LCxD2S<2:0>**: Input Data 2 Selection Control bits(1) |
| 111 | CLCxIN[7] is selected for lcxd2. |
| 110 | CLCxIN[6] is selected for lcxd2. |
| 101 | CLCxIN[5] is selected for lcxd2. |
| 100 | CLCxIN[4] is selected for lcxd2. |
| 011 | CLCxIN[3] is selected for lcxd2. |
| 010 | CLCxIN[2] is selected for lcxd2. |
| 001 | CLCxIN[1] is selected for lcxd2. |
| 000 | CLCxIN[0] is selected for lcxd2. |

| bit 3 | **Unimplemented**: Read as ‘0’ |
| bit 2-0 | **LCxD1S<2:0>**: Input Data 1 Selection Control bits(1) |
| 111 | CLCxIN[7] is selected for lcxd1. |
| 110 | CLCxIN[6] is selected for lcxd1. |
| 101 | CLCxIN[5] is selected for lcxd1. |
| 100 | CLCxIN[4] is selected for lcxd1. |
| 011 | CLCxIN[3] is selected for lcxd1. |
| 010 | CLCxIN[2] is selected for lcxd1. |
| 001 | CLCxIN[1] is selected for lcxd1. |
| 000 | CLCxIN[0] is selected for lcxd1. |

**Note 1:** See Table 19-1 for signal names associated with inputs.
REGISTER 19-4: CLCxSEL1: MULTIPLEXER DATA 3 AND 4 SELECT REGISTER

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6-4</th>
<th>bit 3</th>
<th>bit 2-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>U-0</td>
<td>R/W-x/u</td>
<td>U-0</td>
<td>R/W-x/u</td>
</tr>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>R/W-x/u</td>
<td></td>
<td>R/W-x/u</td>
<td></td>
</tr>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- -n/n = Value at POR and BOR/Value at all other Resets

Note 1: See Table 19-1 for signal names associated with inputs.
### REGISTER 19-5: CLCxGLS0: GATE 1 LOGIC SELECT REGISTER

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCxG1D4T</td>
<td>LCxG1D4N</td>
</tr>
<tr>
<td>LCxG1D4T</td>
<td>LCxG1D4N</td>
</tr>
<tr>
<td>LCxG1D4T</td>
<td>LCxG1D4N</td>
</tr>
<tr>
<td>LCxG1D3T</td>
<td>LCxG1D3N</td>
</tr>
<tr>
<td>LCxG1D3T</td>
<td>LCxG1D3N</td>
</tr>
<tr>
<td>LCxG1D2T</td>
<td>LCxG1D2N</td>
</tr>
<tr>
<td>LCxG1D2T</td>
<td>LCxG1D2N</td>
</tr>
<tr>
<td>LCxG1D1T</td>
<td>LCxG1D1N</td>
</tr>
<tr>
<td>LCxG1D1T</td>
<td>LCxG1D1N</td>
</tr>
</tbody>
</table>

#### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

#### bit 7
- **LCxG1D4T**: Gate 1 Data 4 True (non-inverted) bit
  - **1** = lcxd4T is gated into lcxg1
  - **0** = lcxd4T is not gated into lcxg1

#### bit 6
- **LCxG1D4N**: Gate 1 Data 4 Negated (inverted) bit
  - **1** = lcxd4N is gated into lcxg1
  - **0** = lcxd4N is not gated into lcxg1

#### bit 5
- **LCxG1D3T**: Gate 1 Data 3 True (non-inverted) bit
  - **1** = lcxd3T is gated into lcxg1
  - **0** = lcxd3T is not gated into lcxg1

#### bit 4
- **LCxG1D3N**: Gate 1 Data 3 Negated (inverted) bit
  - **1** = lcxd3N is gated into lcxg1
  - **0** = lcxd3N is not gated into lcxg1

#### bit 3
- **LCxG1D2T**: Gate 1 Data 2 True (non-inverted) bit
  - **1** = lcxd2T is gated into lcxg1
  - **0** = lcxd2T is not gated into lcxg1

#### bit 2
- **LCxG1D2N**: Gate 1 Data 2 Negated (inverted) bit
  - **1** = lcxd2N is gated into lcxg1
  - **0** = lcxd2N is not gated into lcxg1

#### bit 1
- **LCxG1D1T**: Gate 1 Data 1 True (non-inverted) bit
  - **1** = lcxd1T is gated into lcxg1
  - **0** = lcxd1T is not gated into lcxg1

#### bit 0
- **LCxG1D1N**: Gate 1 Data 1 Negated (inverted) bit
  - **1** = lcxd1N is gated into lcxg1
  - **0** = lcxd1N is not gated into lcxg1
## REGISTER 19-6: CLCxGLS1: GATE 2 LOGIC SELECT REGISTER

<table>
<thead>
<tr>
<th>bit 7</th>
<th>LCxG2D4T</th>
<th>LCxG2D4N</th>
<th>LCxG2D3T</th>
<th>LCxG2D3N</th>
<th>LCxG2D2T</th>
<th>LCxG2D2N</th>
<th>LCxG2D1T</th>
<th>LCxG2D1N</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
</tr>
</tbody>
</table>

### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

#### bit 7
- **LCxG2D4T**: Gate 2 Data 4 True (non-inverted) bit
  - 1 = lcxd4T is gated into lcxg2
  - 0 = lcxd4T is not gated into lcxg2

#### bit 6
- **LCxG2D4N**: Gate 2 Data 4 Negated (inverted) bit
  - 1 = lcxd4N is gated into lcxg2
  - 0 = lcxd4N is not gated into lcxg2

#### bit 5
- **LCxG2D3T**: Gate 2 Data 3 True (non-inverted) bit
  - 1 = lcxd3T is gated into lcxg2
  - 0 = lcxd3T is not gated into lcxg2

#### bit 4
- **LCxG2D3N**: Gate 2 Data 3 Negated (inverted) bit
  - 1 = lcxd3N is gated into lcxg2
  - 0 = lcxd3N is not gated into lcxg2

#### bit 3
- **LCxG2D2T**: Gate 2 Data 2 True (non-inverted) bit
  - 1 = lcxd2T is gated into lcxg2
  - 0 = lcxd2T is not gated into lcxg2

#### bit 2
- **LCxG2D2N**: Gate 2 Data 2 Negated (inverted) bit
  - 1 = lcxd2N is gated into lcxg2
  - 0 = lcxd2N is not gated into lcxg2

#### bit 1
- **LCxG2D1T**: Gate 2 Data 1 True (non-inverted) bit
  - 1 = lcxd1T is gated into lcxg2
  - 0 = lcxd1T is not gated into lcxg2

#### bit 0
- **LCxG2D1N**: Gate 2 Data 1 Negated (inverted) bit
  - 1 = lcxd1N is gated into lcxg2
  - 0 = lcxd1N is not gated into lcxg2
### REGISTER 19-7: CLCxGLS2: GATE 3 LOGIC SELECT REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>R/W-x/u</th>
<th>LCxG3D4T</th>
<th>LCxG3D4N</th>
<th>LCxG3D3T</th>
<th>LCxG3D3N</th>
<th>LCxG3D2T</th>
<th>LCxG3D2N</th>
<th>LCxG3D1T</th>
<th>LCxG3D1N</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared

- **bit 7** 
  - **LCxG3D4T**: Gate 3 Data 4 True (non-inverted) bit
    - 1 = lcxd4T is gated into lcxg3
    - 0 = lcxd4T is not gated into lcxg3

- **bit 6** 
  - **LCxG3D4N**: Gate 3 Data 4 Negated (inverted) bit
    - 1 = lcxd4N is gated into lcxg3
    - 0 = lcxd4N is not gated into lcxg3

- **bit 5** 
  - **LCxG3D3T**: Gate 3 Data 3 True (non-inverted) bit
    - 1 = lcxd3T is gated into lcxg3
    - 0 = lcxd3T is not gated into lcxg3

- **bit 4** 
  - **LCxG3D3N**: Gate 3 Data 3 Negated (inverted) bit
    - 1 = lcxd3N is gated into lcxg3
    - 0 = lcxd3N is not gated into lcxg3

- **bit 3** 
  - **LCxG3D2T**: Gate 3 Data 2 True (non-inverted) bit
    - 1 = lcxd2T is gated into lcxg3
    - 0 = lcxd2T is not gated into lcxg3

- **bit 2** 
  - **LCxG3D2N**: Gate 3 Data 2 Negated (inverted) bit
    - 1 = lcxd2N is gated into lcxg3
    - 0 = lcxd2N is not gated into lcxg3

- **bit 1** 
  - **LCxG3D1T**: Gate 3 Data 1 True (non-inverted) bit
    - 1 = lcxd1T is gated into lcxg3
    - 0 = lcxd1T is not gated into lcxg3

- **bit 0** 
  - **LCxG3D1N**: Gate 3 Data 1 Negated (inverted) bit
    - 1 = lcxd1N is gated into lcxg3
    - 0 = lcxd1N is not gated into lcxg3
## REGISTER 19-8: CLCxG3: GATE 4 LOGIC SELECT REGISTER

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCxG4D4T</td>
<td>LCxG4D4N</td>
<td>LCxG4D3T</td>
<td>LCxG4D3N</td>
<td>LCxG4D2T</td>
<td>LCxG4D2N</td>
<td>LCxG4D1T</td>
<td>LCxG4D1N</td>
</tr>
</tbody>
</table>

| Legend: |
|--------|--------|--------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared |

- **bit 7** **LCxG4D4T**: Gate 4 Data 4 True (non-inverted) bit
  - 1 = Icxd4T is gated into Icxg4
  - 0 = Icxd4T is not gated into Icxg4

- **bit 6** **LCxG4D4N**: Gate 4 Data 4 Negated (inverted) bit
  - 1 = Icxd4N is gated into Icxg4
  - 0 = Icxd4N is not gated into Icxg4

- **bit 5** **LCxG4D3T**: Gate 4 Data 3 True (non-inverted) bit
  - 1 = Icxd3T is gated into Icxg4
  - 0 = Icxd3T is not gated into Icxg4

- **bit 4** **LCxG4D3N**: Gate 4 Data 3 Negated (inverted) bit
  - 1 = Icxd3N is gated into Icxg4
  - 0 = Icxd3N is not gated into Icxg4

- **bit 3** **LCxG4D2T**: Gate 4 Data 2 True (non-inverted) bit
  - 1 = Icxd2T is gated into Icxg4
  - 0 = Icxd2T is not gated into Icxg4

- **bit 2** **LCxG4D2N**: Gate 4 Data 2 Negated (inverted) bit
  - 1 = Icxd2N is gated into Icxg4
  - 0 = Icxd2N is not gated into Icxg4

- **bit 1** **LCxG4D1T**: Gate 4 Data 1 True (non-inverted) bit
  - 1 = Icxd1T is gated into Icxg4
  - 0 = Icxd1T is not gated into Icxg4

- **bit 0** **LCxG4D1N**: Gate 4 Data 1 Negated (inverted) bit
  - 1 = Icxd1N is gated into Icxg4
  - 0 = Icxd1N is not gated into Icxg4
### TABLE 19-3: SUMMARY OF REGISTERS ASSOCIATED WITH CLCx

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit7</th>
<th>Bit6</th>
<th>Bit5</th>
<th>Bit4</th>
<th>Bit3</th>
<th>Bit2</th>
<th>Bit1</th>
<th>Bit0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLC1CON</td>
<td>LC1EN</td>
<td>LC1OE</td>
<td>LC1OUT</td>
<td>LC1INTP</td>
<td>LC1INTN</td>
<td>LC1MODE&lt;2:0&gt;</td>
<td></td>
<td></td>
<td>110</td>
</tr>
<tr>
<td>CLC1GLS0</td>
<td>LC1G1D4T</td>
<td>LC1G1D4N</td>
<td>LC1G1D3T</td>
<td>LC1G1D3N</td>
<td>LC1G1D2T</td>
<td>LC1G1D2N</td>
<td>LC1G1D1T</td>
<td>LC1G1D1N</td>
<td>114</td>
</tr>
<tr>
<td>CLC1GLS1</td>
<td>LC1G2D4T</td>
<td>LC1G2D4N</td>
<td>LC1G2D3T</td>
<td>LC1G2D3N</td>
<td>LC1G2D2T</td>
<td>LC1G2D2N</td>
<td>LC1G2D1T</td>
<td>LC1G2D1N</td>
<td>115</td>
</tr>
<tr>
<td>CLC1GLS2</td>
<td>LC1G3D4T</td>
<td>LC1G3D4N</td>
<td>LC1G3D3T</td>
<td>LC1G3D3N</td>
<td>LC1G3D2T</td>
<td>LC1G3D2N</td>
<td>LC1G3D1T</td>
<td>LC1G3D1N</td>
<td>116</td>
</tr>
<tr>
<td>CLC1GLS3</td>
<td>LC1G4D4T</td>
<td>LC1G4D4N</td>
<td>LC1G4D3T</td>
<td>LC1G4D3N</td>
<td>LC1G4D2T</td>
<td>LC1G4D2N</td>
<td>LC1G4D1T</td>
<td>LC1G4D1N</td>
<td>117</td>
</tr>
<tr>
<td>CLC1POL</td>
<td>LC1POL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>LC1G4POL</td>
<td>LC1G3POL</td>
<td>LC1G2POL</td>
<td>LC1G1POL</td>
<td>111</td>
</tr>
<tr>
<td>CLC1SEL0</td>
<td>—</td>
<td>—</td>
<td>LC1D2S&lt;2:0&gt;</td>
<td>—</td>
<td>—</td>
<td>LC1D1S&lt;2:0&gt;</td>
<td>—</td>
<td>—</td>
<td>112</td>
</tr>
<tr>
<td>CLC1SEL1</td>
<td>—</td>
<td>—</td>
<td>LC1D4S&lt;2:0&gt;</td>
<td>—</td>
<td>—</td>
<td>LC1D3S&lt;2:0&gt;</td>
<td>—</td>
<td>—</td>
<td>113</td>
</tr>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>TMR0IE</td>
<td>INTE</td>
<td>IOCIE</td>
<td>TMR0IF</td>
<td>INTF</td>
<td>IOCIF</td>
<td>40</td>
</tr>
<tr>
<td>PIE1</td>
<td>—</td>
<td>ADIE</td>
<td>—</td>
<td>NCO1IE</td>
<td>CLC1IE</td>
<td>—</td>
<td>TMR2IE</td>
<td>—</td>
<td>41</td>
</tr>
<tr>
<td>PIR1</td>
<td>—</td>
<td>ADIF</td>
<td>—</td>
<td>NCO1IF</td>
<td>CLC1IF</td>
<td>—</td>
<td>TMR2IF</td>
<td>—</td>
<td>42</td>
</tr>
<tr>
<td>TRISA</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TRISA2</td>
<td>TRISA1</td>
<td>TRISA0</td>
<td>69</td>
</tr>
</tbody>
</table>

**Legend:** — = unimplemented read as ‘0’. Shaded cells are not used for CLC module.
20.0 NUMERICALLY CONTROLLED OSCILLATOR (NCO) MODULE

The Numerically Controlled Oscillator (NCOx) module is a timer that uses the overflow from the addition of an increment value to divide the input frequency. The advantage of the addition method over simple counter driven timer is that the resolution of division does not vary with the divider value. The NCOx is most useful for applications that requires frequency accuracy and fine resolution at a fixed duty cycle.

Features of the NCOx include:

- 16-bit increment function
- Fixed Duty Cycle (FDC) mode
- Pulse Frequency (PF) mode
- Output pulse width control
- Multiple clock input sources
- Output polarity control
- Interrupt capability

Figure 20-1 is a simplified block diagram of the NCOx module.
FIGURE 20-1: NUMERICALLY CONTROLLED OSCILLATOR (NCOx) MODULE SIMPLIFIED BLOCK DIAGRAM

Note 1: The increment registers are double-buffered to allow for value changes to be made without first disabling the NCO module. The full increment value is loaded into the buffer registers on the second rising edge of the NCOx_clk signal that occurs immediately after a write to NCOxINCL register. The buffers are not user-accessible and are shown here for reference.
20.1 NCOx OPERATION

The NCOx operates by repeatedly adding a fixed value to an accumulator. Additions occur at the input clock rate. The accumulator will overflow with a carry periodically, which is the raw NCOx output. This effectively reduces the input clock by the ratio of the addition value to the maximum accumulator value. See Equation 20-1.

The NCOx output can be further modified by stretching the pulse or toggling a flip-flop. The modified NCOx output is then distributed internally to other peripherals and optionally output to a pin. The accumulator overflow also generates an interrupt.

The NCOx output creates an instantaneous frequency, which may cause uncertainty. This output depends on the ability of the receiving circuit (i.e., CWG or external resonant converter circuitry) to average the instantaneous frequency to reduce uncertainty.

20.1.1 NCOx CLOCK SOURCES

Clock sources available to the NCOx include:
- HFINTOSC
- Fosc
- LC1OUT
- NCO1CLK pin

The NCOx clock source is selected by configuring the NxCKS<1:0> bits in the NCOxCLK register.

20.1.2 ACCUMULATOR

The Accumulator is a 20-bit register. Read and write access to the Accumulator is available through three registers:
- NCOxACCL
- NCOxACCH
- NCOxACCU

20.1.3 ADDER

The NCOx Adder is a full adder, which operates asynchronously to the clock source selected. The addition of the previous result and the increment value replaces the accumulator value on the rising edge of each input clock.

20.1.4 INCREMENT REGISTERS

The Increment value is stored in two 8-bit registers making up a 16-bit increment. In order of LSB to MSB they are:
- NCOxINCL
- NCOxINCH

Both of the registers are readable and writable. The Increment registers are double-buffered to allow for value changes to be made without first disabling the NCOx module.

The buffer loads are immediate when the module is disabled. Writing to the MS register first is necessary because then the buffer is loaded synchronously with the NCOx operation after the write is executed on the lower increment register.

\[
F_{\text{Overflow}} = \frac{NCO\, \text{Clock Frequency} \times \text{Increment Value}}{2^n}
\]

\[n = \text{Accumulator width in bits}\]

Note: The increment buffer registers are not user-accessible.
20.2 FIXED DUTY CYCLE (FDC) MODE

In Fixed Duty Cycle (FDC) mode, every time the Accumulator overflows, the output is toggled. This provides a 50% duty cycle, provided that the increment value remains constant. For more information, see Figure 20-2.

The FDC mode is selected by clearing the NxPFM bit in the NCOxCON register.

20.3 PULSE FREQUENCY (PF) MODE

In Pulse Frequency (PF) mode, every time the Accumulator overflows, the output becomes active for one or more clock periods. See Section 20.3.1 “OUTPUT PULSE WIDTH CONTROL” for more information.

Once the clock period expires, the output returns to an inactive state. This provides a pulsed output.

The output becomes active on the rising clock edge immediately following the overflow event. For more information, see Figure 20-2.

The value of the active and inactive states depends on the Polarity bit, NxPOL in the NCOxCON register.

The PF mode is selected by setting the NxPFM bit in the NCOxCON register.

20.3.1 OUTPUT PULSE WIDTH CONTROL

When operating in PF mode, the active state of the output can vary in width by multiple clock periods. Various pulse widths are selected with the NxPWS<2:0> bits in the NCOxCLK register.

When the selected pulse width is greater than the Accumulator overflow time frame, then NCOx operation is undefined.

20.4 OUTPUT POLARITY CONTROL

The last stage in the NCOx module is the output polarity. The NxPOL bit in the NCOxCON register selects the output polarity. Changing the polarity while the interrupts are enabled will cause an interrupt for the resulting output transition.

The NCOx output can be used internally by source code or other peripherals. This is done by reading the NxOUT (read-only) bit of the NCOxCON register.
FIGURE 20-2: NCO – FIXED DUTY CYCLE (FDC) AND PULSE FREQUENCY MODE (PFM) OUTPUT OPERATION DIAGRAM

- NCOx Clock Source
- NCOx Increment Value
- NCOx Accumulator Value
- NCOx Output FDC Mode
- NCOx Output PF Mode NCOxPWS = 000
- NCOx Output PF Mode NCOxPWS = 001
- NCO_overflow
- NCO_interrupt

Values:
- 00000h
- 04000h
- 08000h
- FC000h
- 00000h
- 04000h
- 08000h
- FC000h
- 00000h
- 04000h
- 08000h
20.5 Interrupts

When the Accumulator overflows, the NCOx Interrupt Flag bit, NCOxIF, of the PIR1 register is set. To enable this interrupt event, the following bits must be set:

- NxE bit of the NCOxCON register
- NCOxIE bit of the PIE1 register
- PEIE bit of the INTCON register
- GIE bit of the INTCON register

The interrupt must be cleared by software by clearing the NCOxIF bit in the Interrupt Service Routine.

20.6 Effects of a Reset

All of the NCOx registers are cleared to zero as the result of a Reset.

20.7 Operation In Sleep

The NCO module operates independently from the system clock and will continue to run during Sleep, provided that the clock source selected remains active.

The HFINTOSC remains active during Sleep when the NCO module is enabled and the HFINTOSC is selected as the clock source, regardless of the system clock source selected.

In other words, if the HFINTOSC is simultaneously selected as the system clock and the NCO clock source, when the NCO is enabled, the CPU will go idle during Sleep, but the NCO will continue to operate and the HFINTOSC will remain active.

This will have a direct effect on the Sleep mode current.
### 20.8 NCOx Control Registers

#### REGISTER 20-1: NCOxCON: NCOx CONTROL REGISTER

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6</th>
<th>bit 5</th>
<th>bit 4</th>
<th>bit 3-1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>NxEN: NCOx Enable bit</td>
<td>NxOE: NCOx Output Enable bit</td>
<td>NxOUT: NCOx Output bit</td>
<td>NxPOL: NCOx Polarity bit</td>
<td>Unimplemented</td>
<td>NxPFM: NCOx Pulse Frequency mode bit</td>
</tr>
<tr>
<td>1 = NCOx module is enabled</td>
<td>1 = NCOx output pin is enabled</td>
<td>1 = NCOx output is high</td>
<td>1 = NCOx output signal is active-low (inverted)</td>
<td></td>
<td>1 = NCOx operates in Pulse Frequency mode</td>
</tr>
<tr>
<td>0 = NCOx module is disabled</td>
<td>0 = NCOx output pin is disabled</td>
<td>0 = NCOx output is low</td>
<td>0 = NCOx output signal is active-high (non-inverted)</td>
<td></td>
<td>0 = NCOx operates in Fixed Duty Cycle mode</td>
</tr>
</tbody>
</table>

#### REGISTER 20-2: NCOxCLK: NCOx INPUT CLOCK CONTROL REGISTER

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6</th>
<th>bit 5</th>
<th>bit 4-2</th>
<th>bit 1-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>NxPWS&lt;2:0&gt;: NCOx Output Pulse Width Select bits</td>
<td>NxCKS&lt;1:0&gt;: NCOx Clock Source Select bits</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

#### Note 1:
- NxPWS applies only when operating in Pulse Frequency mode.
- If NCOx pulse width is greater than NCOx overflow period, operation is undefined.
### REGISTER 20-3: NCOxACCL: NCOx ACCUMULATOR REGISTER – LOW BYTE

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
</tr>
<tr>
<td>NCOxACC&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

**Note 1:** NxPWS applies only when operating in Pulse Frequency mode.

**Note 2:** If NCOx pulse width is greater than NCOx overflow period, operation is undefined.

### REGISTER 20-4: NCOxACCH: NCOx ACCUMULATOR REGISTER – HIGH BYTE

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
</tr>
<tr>
<td>NCOxACC&lt;15:8&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

**bit 7-0** NCOxAC<7:0>: NCOx Accumulator, low byte

**bit 7-0** NCOxAC<15:8>: NCOx Accumulator, high byte

### REGISTER 20-5: NCOxACCU: NCOx ACCUMULATOR REGISTER – UPPER BYTE

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>R/W-0/0</td>
</tr>
<tr>
<td>NCOxACC&lt;19:16&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

**bit 7-4** Unimplemented: Read as ‘0’

**bit 3-0** NCOxAC<19:16>: NCOx Accumulator, upper byte
REGISTER 20-6:  NCOxINCL: NCOx INCREMENT REGISTER – LOW BYTE

<table>
<thead>
<tr>
<th>Bit 7-0</th>
<th>NCOxINC&lt;7:0&gt;: NCOx Increment, low byte</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

REGISTER 20-7:  NCOxINCH: NCOx INCREMENT REGISTER – HIGH BYTE

<table>
<thead>
<tr>
<th>Bit 7-0</th>
<th>NCOxINC&lt;15:8&gt;: NCOx Increment, high byte</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets
### TABLE 20-1: SUMMARY OF REGISTERS ASSOCIATED WITH NCOx

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLC1SEL0</td>
<td>—</td>
<td>LC1D2S2</td>
<td>LC1D2S1</td>
<td>LC1D2S0</td>
<td>—</td>
<td>LC1D1S2</td>
<td>LC1D1S1</td>
<td>LC1D1S0</td>
<td>112</td>
</tr>
<tr>
<td>CLC1SEL1</td>
<td>—</td>
<td>LC1D4S2</td>
<td>LC1D4S1</td>
<td>LC1D4S0</td>
<td>—</td>
<td>LC1D3S2</td>
<td>LC1D3S1</td>
<td>LC1D3S0</td>
<td>113</td>
</tr>
<tr>
<td>CWG1CON1</td>
<td>G1ASDLB&lt;1:0&gt;</td>
<td>G1ASDLA&lt;1:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>G1IS&lt;1:0&gt;</td>
<td></td>
<td></td>
<td>140</td>
</tr>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>TMROIE</td>
<td>INTE</td>
<td>IOCIE</td>
<td>TMROIF</td>
<td>INTF</td>
<td>IOCIF</td>
<td>40</td>
</tr>
<tr>
<td>NCO1ACCH</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>NCO1ACCH&lt;15:8&gt;</td>
<td></td>
<td>126</td>
</tr>
<tr>
<td>NCO1ACCL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>NCO1ACCL&lt;7:0&gt;</td>
<td></td>
<td>126</td>
</tr>
<tr>
<td>NCO1ACCU</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>NCO1ACCU&lt;19:16&gt;</td>
<td></td>
<td>126</td>
</tr>
<tr>
<td>NCO1CLK</td>
<td>N1PWS&lt;2:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>N1CKS&lt;1:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td>125</td>
</tr>
<tr>
<td>NCO1CON</td>
<td>N1EN</td>
<td>N1OE</td>
<td>N1OUT</td>
<td>N1POL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>N1PFM</td>
<td>125</td>
</tr>
<tr>
<td>NCO1INCH</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>NCO1INCH&lt;15:8&gt;</td>
<td></td>
<td>127</td>
</tr>
<tr>
<td>NCO1INCL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>NCO1INCL&lt;7:0&gt;</td>
<td></td>
<td>127</td>
</tr>
<tr>
<td>PIE1</td>
<td>—</td>
<td>ADIE</td>
<td>—</td>
<td>NCO1IE</td>
<td>CLC1IE</td>
<td>—</td>
<td>TMR2IE</td>
<td>—</td>
<td>41</td>
</tr>
<tr>
<td>PIR1</td>
<td>—</td>
<td>ADIF</td>
<td>—</td>
<td>NCO1IF</td>
<td>CLC1IF</td>
<td>—</td>
<td>TMR2IF</td>
<td>—</td>
<td>42</td>
</tr>
<tr>
<td>TRISA</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TRISA2</td>
<td>TRISA1</td>
<td>TRISA0</td>
</tr>
</tbody>
</table>

**Legend:**  
\( x \) = unknown, \( u \) = unchanged, \( -- \) = unimplemented read as ‘0’, \( q \) = value depends on condition. Shaded cells are not used for NCO module.
21.0 COMPLEMENTARY WAVEFORM GENERATOR (CWG) MODULE

The Complementary Waveform Generator (CWG) produces a complementary waveform with dead-band delay from a selection of input sources.

The CWG module has the following features:

- Selectable dead-band clock source control
- Selectable input sources
- Output enable control
- Output polarity control
- Dead-band control with Independent 6-bit rising and falling edge dead-band counters
- Auto-shutdown control with:
  - Selectable shutdown sources
  - Auto-restart enable
  - Auto-shutdown pin override control
FIGURE 21-2: TYPICAL CWG OPERATION WITH PWM1 (NO AUTO-SHUTDOWN)
21.1 Fundamental Operation

The CWG generates a two output complementary waveform from one of four selectable input sources.

The off-to-on transition of each output can be delayed from the on-to-off transition of the other output, thereby, creating a time delay immediately where neither output is driven. This is referred to as dead time and is covered in Section 21.5 “Dead-Band Control”. A typical operating waveform, with dead band, generated from a single input signal is shown in Figure 21-2.

It may be necessary to guard against the possibility of circuit faults or a feedback event arriving too late or not at all. In this case, the active drive must be terminated before the Fault condition causes damage. This is referred to as auto-shutdown and is covered in Section 21.9 “Auto-shutdown Control”.

21.2 Clock Source

The CWG module allows the following clock sources to be selected:
- Fosc (system clock)
- HFINTOSC (16 MHz only)

The clock sources are selected using the G1CS0 bit of the CWGxCON0 register (Register 21-1).

21.3 Selectable Input Sources

The CWG can generate the complementary waveform for the following input sources:
- PWM1
- PWM2
- N1OUT
- L1OUT

The input sources are selected using the GxIS<1:0> bits in the CWGxCON1 register (Register 21-2).

21.4 Output Control

Immediately after the CWG module is enabled, the complementary drive is configured with both CWGxA and CWGxB drives cleared.

21.4.1 OUTPUT ENABLES

Each CWG output pin has individual output enable control. Output enables are selected with the GxOEA and GxOEB bits of the CWGxCON0 register. When an output enable control is cleared, the module asserts no control over the pin. When an output enable is set, the override value or active PWM waveform is applied to the pin per the port priority selection. The output pin enables are dependent on the module enable bit, GxEN. When GxEN is cleared, CWG output enables and CWG drive levels have no effect.

21.4.2 POLARITY CONTROL

The polarity of each CWG output can be selected independently. When the output polarity bit is set, the corresponding output is active-high. Clearing the output polarity bit configures the corresponding output as active-low. However, polarity does not affect the override levels. Output polarity is selected with the GxPOLA and GxPOLB bits of the CWGxCON0 register.

21.5 Dead-Band Control

Dead-band control provides for non-overlapping output signals to prevent shoot-through current in power switches. The CWG contains two 6-bit dead-band counters. One dead-band counter is used for the rising edge of the input source control. The other is used for the falling edge of the input source control.

Dead band is timed by counting CWG clock periods from zero up to the value in the rising or falling dead-band counter registers. See CWGxDBR and CWGxDBF registers (Register 21-4 and Register 21-5, respectively).

21.6 Rising Edge Dead Band

The rising edge dead band delays the turn-on of the CWGxA output from when the CWGxB output is turned off. The rising edge dead-band time starts when the rising edge of the input source signal goes true. When this happens, the CWGxB output is immediately turned off and the rising edge dead-band delay time starts. When the rising edge dead-band delay time is reached, the CWGxA output is turned on.

The CWGxDBR register sets the duration of the dead-band interval on the rising edge of the input source signal. This duration is from 0 to 64 counts of dead band. Dead band is always counted off the edge on the input source signal. A count of 0 (zero), indicates that no dead band is present.

If the input source signal is not present for enough time for the count to be completed, no output will be seen on the respective output.
21.7 Falling Edge Dead Band

The falling edge dead band delays the turn-on of the CWGxB output from when the CWGxA output is turned off. The falling edge dead-band time starts when the falling edge of the input source goes true. When this happens, the CWGxA output is immediately turned off and the falling edge dead-band delay time starts. When the falling edge dead-band delay time is reached, the CWGxB output is turned on.

The CWGxDBF register sets the duration of the dead-band interval on the falling edge of the input source signal. This duration is from 0 to 64 counts of dead band.

Dead band is always counted off the edge on the input source signal. A count of 0 (zero), indicates that no dead band is present.

If the input source signal is not present for enough time for the count to be completed, no output will be seen on the respective output.

Refer to Figure 21-3 and Figure 21-4 for examples.

21.8 Dead-Band Uncertainty

When the rising and falling edges of the input source triggers the dead-band counters, the input may be asynchronous. This will create some uncertainty in the dead-band time delay. The maximum uncertainty is equal to one CWG clock period. Refer to Equation 21-1 for more detail.
FIGURE 21-3: DEAD-BAND OPERATION, CWGxDBR = 01H, CWGxDBF = 02H

- cwg_clock
- Input Source
- CWGxA
- CWGxB

FIGURE 21-4: DEAD-BAND OPERATION, CWGxDBR = 03H, CWGxDBF = 04H, SOURCE SHORTER THAN DEAD BAND

- cwg_clock
- Input Source
- CWGxA
- CWGxB

source shorter than dead band
**EQUATION 21-1:** DEAD-BAND DELAY TIME UNCERTAINTY

\[ T_{DEADBAND\_UNCERTAINTY} = \frac{1}{F_{cwg\_clock}} \]

**EXAMPLE 21-1:** DEAD-BAND DELAY TIME UNCERTAINTY

\[ F_{cwg\_clock} = 16 \text{ MHz} \]

Therefore:

\[ T_{DEADBAND\_UNCERTAINTY} = \frac{1}{F_{cwg\_clock}} = \frac{1}{16 \text{ MHz}} = 625 \text{ ns} \]
21.9 Auto-shutdown Control

Auto-shutdown is a method to immediately override the CWG output levels with specific overrides that allow for safe shutdown of the circuit. The shutdown state can be either cleared automatically or held until cleared by software.

21.9.1 SHUTDOWN

The Shutdown state can be entered by either of the following two methods:

- Software generated
- External Input

21.9.1.1 Software Generated Shutdown

Setting the GxASE bit of the CWGxCON2 register will force the CWG into the shutdown state.

When auto-restart is disabled, the shutdown state will persist as long as the GxASE bit is set.

When auto-restart is enabled, the GxASE bit will clear automatically and resume operation on the next rising edge event. See Figure 21-6.

21.9.1.2 External Input Source

External shutdown inputs provide the fastest way to safely suspend CWG operation in the event of a Fault condition. When any of the selected shutdown inputs goes high, the CWG outputs will immediately go to the selected override levels without software delay. Any combination of two input sources can be selected to cause a shutdown condition. The two sources are:

- LC1OUT
- CWG1FLT

Shutdown inputs are selected using the GxASDS0 and GxASDS1 bits of the CWGxCON2 register. (Register 21-3).

Note: Shutdown inputs are level sensitive, not edge sensitive. The shutdown state cannot be cleared, except by disabling auto-shutdown, as long as the shutdown input level persists.

21.10 Operation During Sleep

The CWG module operates independently from the system clock and will continue to run during Sleep, provided that the clock and input sources selected remain active.

The HFINTOSC remains active during Sleep, provided that the CWG module is enabled, the input source is active, and the HFINTOSC is selected as the clock source, regardless of the system clock source selected.

In other words, if the HFINTOSC is simultaneously selected as the system clock and the CWG clock source, when the CWG is enabled and the input source is active, the CPU will go idle during Sleep, but the CWG will continue to operate and the HFINTOSC will remain active.

This will have a direct effect on the Sleep mode current.
21.11 Configuring the CWG

The following steps illustrate how to properly configure the CWG to ensure a synchronous start:

1. Ensure that the TRIS control bits corresponding to CWGxA and CWGxB are set so that both are configured as inputs.
2. Clear the GxEN bit, if not already cleared.
3. Set desired dead-band times with the CWGxDBR and CWGxDBF registers.
4. Setup the following controls in CWGxCON2 auto-shutdown register:
   • Select desired shutdown source.
   • Select both output overrides to the desired levels (this is necessary even if not using auto-shutdown because start-up will be from a shutdown state).
   • Set the GxASE bit and clear the GxARSEN bit.
5. Select the desired input source using the CWGxCON1 register.
6. Configure the following controls in CWGxCON0 register:
   • Select desired clock source.
   • Select the desired output polarities.
   • Set the output enables for the outputs to be used.
7. Set the GxEN bit.
8. Clear TRIS control bits corresponding to CWGxA and CWGxB to be used to configure those pins as outputs.
9. If auto-restart is to be used, set the GxARSEN bit and the GxASE bit will be cleared automatically. Otherwise, clear the GxASE bit to start the CWG.

21.11.1 PIN OVERRIDE LEVELS

The levels driven to the output pins, while the shutdown input is true, are controlled by the GxASDLA and GxASDLB bits of the CWGxCON1 register (Register 21-2). GxASDLA controls the CWG1A override level and GxASDLB controls the CWG1B override level. The control bit logic level corresponds to the output logic drive level while in the shutdown state. The polarity control does not apply to the override level.

21.11.2 AUTO-SHUTDOWN RESTART

After an auto-shutdown event has occurred, there are two ways to have resume operation:

• Software controlled
• Auto-restart

The restart method is selected with the GxARSEN bit of the CWGxCON2 register. Waveforms of software controlled and automatic restarts are shown in Figure 21-5 and Figure 21-6.
FIGURE 21-5: SHUTDOWN FUNCTIONALITY, AUTO-RESTART DISABLED (GxARSEN = 0)

- CWG Input Source
- Shutdown Source
- GxASE
- CWG1A
- CWG1B

- No Shutdown
- Shutdown Event Ceases
- GxASE Cleared by Software

FIGURE 21-6: SHUTDOWN FUNCTIONALITY, AUTO-RESTART ENABLED (GxARSEN = 1)

- CWG Input Source
- Shutdown Source
- GxASE
- CWG1A
- CWG1B

- No Shutdown
- Shutdown Event Ceases
- GxASE auto-cleared by hardware

- Output Resumes
### 21.12 CWG Control Registers

#### REGISTER 21-1: CWGxCON0: CWG CONTROL REGISTER 0

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2-1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>GxEN</td>
<td>GxOEB</td>
<td>GxOEA</td>
<td>GxPOLB</td>
<td>GxPOLA</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- q = Value depends on condition

- **bit 7**  
  - **GxEN**: CWGx Enable bit  
    - 1 = Module is enabled  
    - 0 = Module is disabled  

- **bit 6**  
  - **GxOEB**: CWGxB Output Enable bit  
    - 1 = CWGxB is available on appropriate I/O pin  
    - 0 = CWGxB is not available on appropriate I/O pin  

- **bit 5**  
  - **GxOEA**: CWGxA Output Enable bit  
    - 1 = CWGxA is available on appropriate I/O pin  
    - 0 = CWGxA is not available on appropriate I/O pin  

- **bit 4**  
  - **GxPOLB**: CWGxB Output Polarity bit  
    - 1 = Output is inverted polarity  
    - 0 = Output is normal polarity  

- **bit 3**  
  - **GxPOLA**: CWGxA Output Polarity bit  
    - 1 = Output is inverted polarity  
    - 0 = Output is normal polarity  

- **bit 2-1**  
  - **Unimplemented**: Read as ‘0’  

- **bit 0**  
  - **GxCS0**: CWGx Clock Source Select bit  
    - 1 = HFINTOSC  
    - 0 = FOSC
REGISTER 21-2: CWGxCON1: CWG CONTROL REGISTER 1

<table>
<thead>
<tr>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>GxASDLB&lt;1:0&gt;</td>
<td>GxASDLA&lt;1:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>GxIS&lt;1:0&gt;</td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared
- q = Value depends on condition

bit 7-6  **GxASDLB<1:0>:** CWGx Shutdown State for CWGxB  
When an auto shutdown event is present (GxASE = 1):
- 11 = CWGxB pin is driven to '1', regardless of the setting of the GxPOLB bit.
- 10 = CWGxB pin is driven to '0', regardless of the setting of the GxPOLB bit.
- 01 = CWGxB pin is tri-stated
- 00 = CWGxB pin is driven to its inactive state after the selected dead-band interval. GxPOLB still will control the polarity of the output.

bit 5-4  **GxASDLA<1:0>:** CWGx Shutdown State for CWGxA  
When an auto shutdown event is present (GxASE = 1):
- 00 = CWGxA pin is driven to its inactive state after the selected dead-band interval. GxPOLA still will control the polarity of the output.
- 01 = CWGxA pin is tri-stated
- 10 = CWGxA pin is driven to '0', regardless of the setting of the GxPOLA bit.
- 11 = CWGxA pin is driven to '1', regardless of the setting of the GxPOLA bit.

bit 3-2  **Unimplemented:** Read as '0'

bit 1-0  **GxIS<1:0>:** CWGx Dead-band Source Select bits
- 11 = LC1OUT
- 10 = N1OUT
- 01 = PWM2OUT
- 00 = PWM1OUT
**REGISTER 21-3: CWGxCON2: CWG CONTROL REGISTER 2**

<table>
<thead>
<tr>
<th>Bit</th>
<th>GxASE</th>
<th>GxARSEN</th>
<th>GxASDCLC1</th>
<th>GxASDFLT</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5-2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**

- **HC** = Bit is cleared by hardware
- **HS** = Bit is set by hardware
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **q** = Value depends on condition

- **bit 7 GxASE**: Auto-Shutdown Event Status bit
  - 1 = An Auto-Shutdown event has occurred. GxOEB/GxOEA Output Controls overridden, Outputs disabled.
  - 0 = No Auto-Shutdown event has occurred, or an Auto-restart has occurred. GxOEB/GxOEA Output Controls enabled.

- **bit 6 GxARSEN**: Auto-Restart Enable bit
  - 1 = Auto-restart is enabled
  - 0 = Auto-restart is disabled

- **bit 5-2 Unimplemented**: Read as ‘0’

- **bit 1 GxASDCLC1**: CWG Auto-shutdown Source Enable bit 1
  - 1 = Shutdown when LC1OUT is high
  - 0 = LC1OUT has no effect on shutdown

- **bit 0 GxASDFLT**: CWG Auto-shutdown Source Enable bit 0
  - 1 = Shutdown when CWG1FLT input is low
  - 0 = CWG1FLT input has no effect on shutdown
### REGISTER 21-4: \texttt{CWGxDBR}: COMPLEMENTARY WAVEFORM GENERATOR (CWGx) RISING DEAD-BAND COUNT REGISTER

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 0</th>
<th>bit 5-0 (\text{CWGxDBR&lt;5:0&gt;}: ) Complementary Waveform Generator (CWGx) Rising Counts bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unimplemented: Read as ‘0’</td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 5-0 (\text{CWGxDBR&lt;5:0&gt;} = )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11 1111 = 63-64 counts of dead band</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11 1110 = 62-63 counts of dead band</td>
<td></td>
<td></td>
</tr>
<tr>
<td>00 0010 = 2-3 counts of dead band</td>
<td></td>
<td></td>
</tr>
<tr>
<td>00 0001 = 1-2 counts of dead band</td>
<td></td>
<td></td>
</tr>
<tr>
<td>00 0000 = 0 counts of dead band</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### REGISTER 21-5: \texttt{CWGxDBF}: COMPLEMENTARY WAVEFORM GENERATOR (CWGx) FALLING DEAD-BAND COUNT REGISTER

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 0</th>
<th>bit 5-0 (\text{CWGxDBF&lt;5:0&gt;}: ) Complementary Waveform Generator (CWGx) Falling Counts bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unimplemented: Read as ‘0’</td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 5-0 (\text{CWGxDBF&lt;5:0&gt; =})</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11 1111 = 63-64 counts of dead band</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11 1110 = 62-63 counts of dead band</td>
<td></td>
<td></td>
</tr>
<tr>
<td>00 0010 = 2-3 counts of dead band</td>
<td></td>
<td></td>
</tr>
<tr>
<td>00 0001 = 1-2 counts of dead band</td>
<td></td>
<td></td>
</tr>
<tr>
<td>00 0000 = 0 counts of dead band. Dead-band generation is bypassed.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### TABLE 21-1: SUMMARY OF REGISTERS ASSOCIATED WITH CWG

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANSELA</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ANSA2</td>
<td>ANSA1</td>
<td>ANSA0</td>
</tr>
<tr>
<td>CWG1CON0</td>
<td>G1EN</td>
<td>G1OEB</td>
<td>G1OEA</td>
<td>G1POLB</td>
<td>G1POLA</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>139</td>
</tr>
<tr>
<td>CWG1CON1</td>
<td>G1ASDLB&lt;1:0&gt;</td>
<td>G1ASDLA&lt;1:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>G1IS&lt;1:0&gt;</td>
<td>140</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CWG1CON2</td>
<td>G1ASE</td>
<td>G1ARSEN</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>141</td>
</tr>
<tr>
<td>CWG1DBF</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>142</td>
</tr>
<tr>
<td>CWG1DBR</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>142</td>
</tr>
<tr>
<td>LATA</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>LATA2</td>
<td>LATA1</td>
<td>LATA0</td>
</tr>
<tr>
<td>TRISA</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TRISA2</td>
<td>TRISA1</td>
<td>TRISA0</td>
</tr>
</tbody>
</table>

**Legend:**  
- x = unknown, u = unchanged, – = unimplemented locations read as ‘0’. Shaded cells are not used by CWG.
22.0 IN-CIRCUIT SERIAL PROGRAMMING™ (ICSP™)

ICSP™ programming allows customers to manufacture circuit boards with unprogrammed devices. Programming can be done after the assembly process allowing the device to be programmed with the most recent firmware or a custom firmware. Five pins are needed for ICSP™ programming:

- ICSPCLK
- ICSPDAT
- MCLR/VPP
- VDD
- VSS

In Program/Verify mode the Program Memory, User IDs and the Configuration Words are programmed through serial communications. The ICSPDAT pin is a bidirectional I/O used for transferring the serial data and the ICSPCLK pin is the clock input. For more information on ICSP™ refer to the “PIC10(L)F320/322 Flash Memory Programming Specification” (DS41572).

22.1 High-Voltage Programming Entry Mode

The device is placed into High-Voltage Programming Entry mode by holding the ICSPCLK and ICSPDAT pins low then raising the voltage on MCLR/VPP to VHH.

22.2 Low-Voltage Programming Entry Mode

The Low-Voltage Programming Entry mode allows the PIC® Flash MCUs to be programmed using VDD only, without high voltage. When the LVP bit of Configuration Word is set to ‘1’, the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to ‘0’.

Entry into the Low-Voltage Programming Entry mode requires the following steps:

1. MCLR is brought to VIL.
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

Once the key sequence is complete, MCLR must be held at VIL for as long as Program/Verify mode is to be maintained.

If low-voltage programming is enabled (LVP = 1), the MCLR Reset function is automatically enabled and cannot be disabled. See Section 5.4 “Low-Power Brown-out Reset (LPBOR)” for more information.

The LVP bit can only be reprogrammed to ‘0’ by using the High-Voltage Programming mode.

22.3 Common Programming Interfaces

Connection to a target device is typically done through an ICSP™ header. A commonly found connector on development tools is the RJ-11 in the 6P6C (6-pin, 6 connector) configuration. See Figure 22-1.

![ICD RJ-11 Style Connector Interface](image)

Another connector often found in use with the PICkit™ programmers is a standard 6-pin header with 0.1 inch spacing. Refer to Figure 22-2.

<table>
<thead>
<tr>
<th>Pin Description*</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 = VPP/MCLR</td>
</tr>
<tr>
<td>2 = VDD Target</td>
</tr>
<tr>
<td>3 = VSS (ground)</td>
</tr>
<tr>
<td>4 = ICSPDAT</td>
</tr>
<tr>
<td>5 = ICSPCLK</td>
</tr>
<tr>
<td>6 = No Connect</td>
</tr>
</tbody>
</table>
FIGURE 22-2: PICkit™ STYLE CONNECTOR INTERFACE

* The 6-pin header (0.100" spacing) accepts 0.025" square pins.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VPP/MCLR</td>
</tr>
<tr>
<td>2</td>
<td>VDD Target</td>
</tr>
<tr>
<td>3</td>
<td>VSS (ground)</td>
</tr>
<tr>
<td>4</td>
<td>ICSPDAT</td>
</tr>
<tr>
<td>5</td>
<td>ICSPCLK</td>
</tr>
<tr>
<td>6</td>
<td>No Connect</td>
</tr>
</tbody>
</table>

Pin 1 Indicator
For additional interface recommendations, refer to your specific device programmer manual prior to PCB design.

It is recommended that isolation devices be used to separate the programming pins from other circuitry. The type of isolation is highly dependent on the specific application and may include devices such as resistors, diodes, or even jumpers. See Figure 22-3 for more information.

**FIGURE 22-3: TYPICAL CONNECTION FOR ICSP™ PROGRAMMING**

![Diagram of ICSP™ Programming Connection](image-url)

- VDD
- VPP
- VSS
- Data
- Clock

* Isolation devices (as required).
23.0 INSTRUCTION SET SUMMARY

The PIC10(L)F320/322 instruction set is highly orthogonal and is comprised of three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each PIC16 instruction is a 14-bit word divided into an **opcode**, which specifies the instruction type and one or more operands, which further specify the operation of the instruction. The formats for each of the categories is presented in **Figure 23-1**, while the various opcode fields are summarized in **Table 23-1**.

**Table 23-2** lists the instructions recognized by the MPASM™ assembler.

For **byte-oriented** instructions, ‘f’ represents a file register designator and ‘d’ represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If ‘d’ is zero, the result is placed in the W register. If ‘d’ is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, ‘b’ represents a bit field designator, which selects the bit affected by the operation, while ‘f’ represents the address of the file in which the bit is located.

For **literal and control** operations, ‘k’ represents an 8-bit or 11-bit constant, or literal value.

One instruction cycle consists of four oscillator periods; for an oscillator frequency of 4 MHz, this gives a normal instruction execution time of 1 µs. All instructions are executed within a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of an instruction. When this occurs, the execution takes two instruction cycles, with the second cycle executed as a **NOP**.

All instruction examples use the format ‘0xhh’ to represent a hexadecimal number, where ‘h’ signifies a hexadecimal digit.

23.1 Read-Modify-Write Operations

Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (RMW) operation. The register is read, the data is modified, and the result is stored according to either the instruction or the destination designator ‘d’. A read operation is performed on a register even if the instruction writes to that register.

For example, a **CLR PORTA** instruction will read PORTA, clear all the data bits, then write the result back to PORTA. This example would have the unintended consequence of clearing the condition that set the IOCF flag.

### TABLE 23-1: OPCODE FIELD DESCRIPTIONS

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>f</td>
<td>Register file address (0x00 to 0x7F)</td>
</tr>
<tr>
<td>W</td>
<td>Working register (accumulator)</td>
</tr>
<tr>
<td>b</td>
<td>Bit address within an 8-bit file register</td>
</tr>
<tr>
<td>k</td>
<td>Literal field, constant data or label</td>
</tr>
<tr>
<td>x</td>
<td>Don’t care location (= 0 or 1). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.</td>
</tr>
<tr>
<td>d</td>
<td>Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1.</td>
</tr>
<tr>
<td>PC</td>
<td>Program Counter</td>
</tr>
<tr>
<td>TO</td>
<td>Time-out bit</td>
</tr>
<tr>
<td>C</td>
<td>Carry bit</td>
</tr>
<tr>
<td>DC</td>
<td>Digit carry bit</td>
</tr>
<tr>
<td>Z</td>
<td>Zero bit</td>
</tr>
<tr>
<td>PD</td>
<td>Power-down bit</td>
</tr>
</tbody>
</table>

### FIGURE 23-1: GENERAL FORMAT FOR INSTRUCTIONS

**Byte-oriented file register operations**

<table>
<thead>
<tr>
<th>13</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
</tr>
<tr>
<td>7</td>
</tr>
<tr>
<td>6</td>
</tr>
<tr>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>OPCODE</th>
<th>d</th>
<th>f (FILE #)</th>
</tr>
</thead>
<tbody>
<tr>
<td>d = 0 for destination W</td>
<td>d = 1 for destination f</td>
<td></td>
</tr>
<tr>
<td>f = 7-bit file register address</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bit-oriented file register operations**

<table>
<thead>
<tr>
<th>13</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
</tr>
<tr>
<td>9</td>
</tr>
<tr>
<td>7</td>
</tr>
<tr>
<td>6</td>
</tr>
<tr>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>OPCODE</th>
<th>b (BIT #)</th>
<th>f (FILE #)</th>
</tr>
</thead>
<tbody>
<tr>
<td>b = 3-bit bit address</td>
<td></td>
<td></td>
</tr>
<tr>
<td>f = 7-bit file register address</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Literal and control operations**

**General**

<table>
<thead>
<tr>
<th>13</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
</tr>
<tr>
<td>7</td>
</tr>
<tr>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>OPCODE</th>
<th>k (literal)</th>
</tr>
</thead>
<tbody>
<tr>
<td>k = 8-bit immediate value</td>
<td></td>
</tr>
</tbody>
</table>

**CALL and GOTO instructions only**

<table>
<thead>
<tr>
<th>13</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
</tr>
<tr>
<td>10</td>
</tr>
<tr>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>OPCODE</th>
<th>k (literal)</th>
</tr>
</thead>
<tbody>
<tr>
<td>k = 11-bit immediate value</td>
<td></td>
</tr>
</tbody>
</table>
### TABLE 23-2: INSTRUCTION SET

<table>
<thead>
<tr>
<th>Mnemonic, Operands</th>
<th>Description</th>
<th>Cycles</th>
<th>14-Bit Opcode MSb</th>
<th>14-Bit Opcode LSb</th>
<th>Status Affected Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>BYTE-ORIENTED FILE REGISTER OPERATIONS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADDWF f, d</td>
<td>Add W and f</td>
<td>1</td>
<td>00 0111 dfff ffff</td>
<td>C, DC, Z</td>
<td>1, 2</td>
</tr>
<tr>
<td>ANDWF f, d</td>
<td>AND W with f</td>
<td>1</td>
<td>00 0101 dfff ffff</td>
<td>Z</td>
<td>1, 2</td>
</tr>
<tr>
<td>CLRF f</td>
<td>Clear f</td>
<td>1</td>
<td>00 0001 lfff ffff</td>
<td>Z</td>
<td>2</td>
</tr>
<tr>
<td>CLRW –</td>
<td>Clear W</td>
<td>1</td>
<td>00 0001 0xxx xxxx</td>
<td>Z</td>
<td></td>
</tr>
<tr>
<td>COMF f, d</td>
<td>Complement f</td>
<td>1</td>
<td>00 1001 dfff ffff</td>
<td>Z</td>
<td>1, 2</td>
</tr>
<tr>
<td>DECf f, d</td>
<td>Decrement f</td>
<td>1</td>
<td>00 0111 dfff ffff</td>
<td>Z</td>
<td>1, 2</td>
</tr>
<tr>
<td>DECFSZ f, d</td>
<td>Decrement f, Skip if 0</td>
<td>1(2)</td>
<td>00 1011 dfff ffff</td>
<td>Z</td>
<td>1, 2, 3</td>
</tr>
<tr>
<td>INCf f, d</td>
<td>Increment f</td>
<td>1</td>
<td>00 1010 dfff ffff</td>
<td>Z</td>
<td>1, 2</td>
</tr>
<tr>
<td>INCFSZ f, d</td>
<td>Increment f, Skip if 0</td>
<td>1(2)</td>
<td>00 1111 dfff ffff</td>
<td>Z</td>
<td>1, 2, 3</td>
</tr>
<tr>
<td>IORWF f, d</td>
<td>Inclusive OR W with f</td>
<td>1</td>
<td>00 0100 dfff ffff</td>
<td>Z</td>
<td>1, 2</td>
</tr>
<tr>
<td>MOVf f, d</td>
<td>Move f</td>
<td>1</td>
<td>00 1000 dfff ffff</td>
<td>Z</td>
<td>1, 2</td>
</tr>
<tr>
<td>MOVWF f</td>
<td>Move W to f</td>
<td>1</td>
<td>00 0000 lfff ffff</td>
<td>Z</td>
<td>1, 2</td>
</tr>
<tr>
<td>NOP –</td>
<td>No Operation</td>
<td></td>
<td>00 0000 0xxx xxxx</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RLF f, d</td>
<td>Rotate Left f through Carry</td>
<td>1</td>
<td>00 1101 dfff ffff</td>
<td>C</td>
<td>1, 2</td>
</tr>
<tr>
<td>RRF f, d</td>
<td>Rotate Right f through Carry</td>
<td>1</td>
<td>00 1100 dfff ffff</td>
<td>C</td>
<td>1, 2</td>
</tr>
<tr>
<td>SUBWF f, d</td>
<td>Subtract W from f</td>
<td>1</td>
<td>00 0110 dfff ffff</td>
<td>C, DC, Z</td>
<td>1, 2</td>
</tr>
<tr>
<td>SWAPF f, d</td>
<td>Swap nibbles in f</td>
<td>1</td>
<td>00 1110 dfff ffff</td>
<td>Z</td>
<td>1, 2</td>
</tr>
<tr>
<td>XORWF f, d</td>
<td>Exclusive OR W with f</td>
<td>1</td>
<td>00 0110 dfff ffff</td>
<td>Z</td>
<td>1, 2</td>
</tr>
<tr>
<td><strong>BIT-ORIENTED FILE REGISTER OPERATIONS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BCF f, b</td>
<td>Bit Clear f</td>
<td>1</td>
<td>01 00bb bfff ffff</td>
<td></td>
<td>1, 2</td>
</tr>
<tr>
<td>BSF f, b</td>
<td>Bit Set f</td>
<td>1</td>
<td>01 01bb bfff ffff</td>
<td></td>
<td>1, 2</td>
</tr>
<tr>
<td>BTFSC f, b</td>
<td>Bit Test f, Skip if Clear</td>
<td>1(2)</td>
<td>01 10bb bfff ffff</td>
<td></td>
<td>3</td>
</tr>
<tr>
<td>BTFSS f, b</td>
<td>Bit Test f, Skip if Set</td>
<td>1(2)</td>
<td>01 11bb bfff ffff</td>
<td></td>
<td>3</td>
</tr>
<tr>
<td><strong>LITERAL AND CONTROL OPERATIONS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADDLW k</td>
<td>Add literal and W</td>
<td>1</td>
<td>11 111x kkkk kkkk</td>
<td>C, DC, Z</td>
<td></td>
</tr>
<tr>
<td>ANDLW k</td>
<td>AND literal with W</td>
<td>1</td>
<td>11 1001 kkkk kkkk</td>
<td>Z</td>
<td></td>
</tr>
<tr>
<td>CALL k</td>
<td>Call Subroutine</td>
<td>2</td>
<td>10 0kkk kkkk kkkk</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLRWDT –</td>
<td>Clear Watchdog Timer</td>
<td>1</td>
<td>00 0000 0110 0100</td>
<td>TO, PD</td>
<td></td>
</tr>
<tr>
<td>GOTO k</td>
<td>Go to address</td>
<td>2</td>
<td>10 1kkk kkkk kkkk</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IORLW k</td>
<td>Inclusive OR literal with W</td>
<td>1</td>
<td>11 1000 kkkk kkkk</td>
<td>Z</td>
<td></td>
</tr>
<tr>
<td>MOVLW k</td>
<td>Move literal to W</td>
<td>1</td>
<td>11 00xx kkkk kkkk</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RETFIE –</td>
<td>Return from interrupt</td>
<td>2</td>
<td>00 0000 0000 1001</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RETLW k</td>
<td>Return with literal in W</td>
<td>2</td>
<td>11 01xx kkkk kkkk</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RETURN –</td>
<td>Return from Subroutine</td>
<td>2</td>
<td>00 0000 0000 1000</td>
<td>TO, PD</td>
<td></td>
</tr>
<tr>
<td>SLEEP –</td>
<td>Go into Standby mode</td>
<td>1</td>
<td>00 0000 0110 0111</td>
<td>TO, PD</td>
<td></td>
</tr>
<tr>
<td>SUBLW k</td>
<td>Subtract W from literal</td>
<td>1</td>
<td>11 110x kkkk kkkk</td>
<td>C, DC, Z</td>
<td></td>
</tr>
<tr>
<td>XORLW k</td>
<td>Exclusive OR literal with W</td>
<td>1</td>
<td>11 1010 kkkk kkkk</td>
<td>Z</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** When an I/O register is modified as a function of itself (e.g., MOVF PORTA, 1), the value used will be that value present on the pins themselves. For example, if the data latch is ‘1’ for a pin configured as input and is driven low by an external device, the data will be written back with a ‘0’.

**Note 2:** If this instruction is executed on the TMR0 register (and where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.

**Note 3:** If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.
### 23.2 Instruction Descriptions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
</table>
| **ADDLW** Add literal and W  
Syntax: \[
\text{[label] ADDLW } k
\]  
Operands: \[0 \leq k \leq 255\]  
Operation: \[(W) + k \rightarrow (W)\]  
Status Affected: C, DC, Z  
Description: The contents of the W register are added to the 8-bit literal 'k' and the result is placed in the W register. |  
**BCF** Bit Clear f  
Syntax: \[
\text{[label] BCF } f,b
\]  
Operands: \[0 \leq f \leq 127\]  
Operation: \[0 \rightarrow (f<b>)\]  
Status Affected: None  
Description: Bit 'b' in register 'f' is cleared. |
| **ADDFWF** Add W and f  
Syntax: \[
\text{[label] ADDWF } f,d
\]  
Operands: \[0 \leq f \leq 127\]  
\[d \in [0,1]\]  
Operation: \[(W) + (f) \rightarrow (destination)\]  
Status Affected: C, DC, Z  
Description: Add the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'. |  
**BSF** Bit Set f  
Syntax: \[
\text{[label] BSF } f,b
\]  
Operands: \[0 \leq f \leq 127\]  
\[0 \leq b \leq 7\]  
Operation: \[1 \rightarrow (f<b>)\]  
Status Affected: None  
Description: Bit 'b' in register 'f' is set. |
| **ANDLW** AND literal with W  
Syntax: \[
\text{[label] ANDLW } k
\]  
Operands: \[0 \leq k \leq 255\]  
Operation: \[(W) .AND. (k) \rightarrow (W)\]  
Status Affected: Z  
Description: The contents of W register are AND'ed with the 8-bit literal 'k'. The result is placed in the W register. |  
**BTFSC** Bit Test f, Skip if Clear  
Syntax: \[
\text{[label] BTFSC } f,b
\]  
Operands: \[0 \leq f \leq 127\]  
\[0 \leq b \leq 7\]  
Operation: \[\text{skip if } (f<b>) = 0\]  
Status Affected: None  
Description: If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b' in register 'f' is '0', the next instruction is discarded, and a NOP is executed instead, making this a 2-cycle instruction. |
| **ANDWF** AND W with f  
Syntax: \[
\text{[label] ANDWF } f,d
\]  
Operands: \[0 \leq f \leq 127\]  
\[d \in [0,1]\]  
Operation: \[(W) .AND. (f) \rightarrow (destination)\]  
Status Affected: Z  
Description: AND the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'. |
**BTFSS**  
**Bit Test f, Skip if Set**  

Syntax:  
```
[ label ] BTFSS f,b
```

Operands:  
- `0 ≤ f ≤ 127`
- `0 ≤ b < 7`

Operation:  
- `skip if (f<b) = 1`

Status Affected:  
None

Description:  
If bit 'b' in register 'f' is '0', the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a **NOP** is executed instead, making this a 2-cycle instruction.

---

**CALL**  
**Call Subroutine**  

Syntax:  
```
[ label ] CALL k
```

Operands:  
- `0 ≤ k ≤ 2047`

Operation:  
- `(PC)+ 1 → TOS`
- `k → PC<10:0>`
- `(PCLATH<4:3>) → PC<12:11>`

Status Affected:  
None

Description:  
Call Subroutine. First, return address (PC + 1) is pushed onto the stack. The 11-bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. **CALL** is a 2-cycle instruction.

---

**CLRF**  
**Clear f**  

Syntax:  
```
[ label ] CLRF f
```

Operands:  
- `0 ≤ f ≤ 127`

Operation:  
- `00h → (f)`
- `1 → Z`

Status Affected:  
Z

Description:  
The contents of register 'f' are cleared and the Z bit is set.

---

**CLRW**  
**Clear W**  

Syntax:  
```
[ label ] CLRW
```

Operands:  
None

Operation:  
- `00h → (W)`
- `1 → Z`

Status Affected:  
Z

Description:  
The W register is cleared. Zero bit (Z) is set.

---

**CLRWDT**  
**Clear Watchdog Timer**  

Syntax:  
```
[ label ] CLRWDT
```

Operands:  
None

Operation:  
- `00h → WDT`
- `0 → WDT prescaler`
- `1 → TO`
- `1 → PD`

Status Affected:  
TO, PD

Description:  
**CLRWDT** instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits TO and PD are set.

---

**COMF**  
**Complement f**  

Syntax:  
```
[ label ] COMF f,d
```

Operands:  
- `0 ≤ f ≤ 127`
- `d ∈ [0,1]`

Operation:  
- `(f) → (destination)`

Status Affected:  
Z

Description:  
The contents of register 'f' are complemented. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'.

---

**DECF**  
**Decrement f**  

Syntax:  
```
[ label ] DECF f,d
```

Operands:  
- `0 ≤ f ≤ 127`
- `d ∈ [0,1]`

Operation:  
- `(f) - 1 → (destination)`

Status Affected:  
Z

Description:  
Decrement register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

---
### DECFSZ

**Decrement f, Skip if 0**

<table>
<thead>
<tr>
<th>Syntax:</th>
<th><code>[ label ] DECFSZ f,d</code></th>
</tr>
</thead>
</table>
| Operands: | $0 \leq f \leq 127$  
$ d \in \{0,1\}$ |
| Operation: | $(f) - 1 \rightarrow \text{(destination)}$  
skip if result = 0 |
| Status Affected: | None |
| Description: | The contents of register ‘f’ are decremented. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’.  
If the result is ‘1’, the next instruction is executed. If the result is ‘0’, a NOP is executed instead, making it a 2-cycle instruction. |

### INCF

**Increment f**

<table>
<thead>
<tr>
<th>Syntax:</th>
<th><code>[ label ] INCF f,d</code></th>
</tr>
</thead>
</table>
| Operands: | $0 \leq f \leq 127$  
$ d \in \{0,1\}$ |
| Operation: | $(f) + 1 \rightarrow \text{(destination)}$ |
| Status Affected: | Z |
| Description: | The contents of register ‘f’ are incremented. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’. |

### INCFSZ

**Increment f, Skip if 0**

<table>
<thead>
<tr>
<th>Syntax:</th>
<th><code>[ label ] INCFSZ f,d</code></th>
</tr>
</thead>
</table>
| Operands: | $0 \leq f \leq 127$  
$ d \in \{0,1\}$ |
| Operation: | $(f) + 1 \rightarrow \text{(destination)}$  
skip if result = 0 |
| Status Affected: | None |
| Description: | The contents of register ‘f’ are incremented. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’.  
If the result is ‘1’, the next instruction is executed. If the result is ‘0’, a NOP is executed instead, making it a 2-cycle instruction. |

### GOTO

**Unconditional Branch**

<table>
<thead>
<tr>
<th>Syntax:</th>
<th><code>[ label ] GOTO k</code></th>
</tr>
</thead>
<tbody>
<tr>
<td>Operands:</td>
<td>$0 \leq k \leq 2047$</td>
</tr>
</tbody>
</table>
| Operation: | $k \rightarrow \text{PC}<10:0>$  
PCLATH<4:3> → PC<12:11> |
| Status Affected: | None |
| Description: | GOTO is an unconditional branch. The 11-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a 2-cycle instruction. |

### IORLW

**Inclusive OR literal with W**

<table>
<thead>
<tr>
<th>Syntax:</th>
<th><code>[ label ] IORLW k</code></th>
</tr>
</thead>
<tbody>
<tr>
<td>Operands:</td>
<td>$0 \leq k \leq 255$</td>
</tr>
<tr>
<td>Operation:</td>
<td>$(W) \ .OR. k \rightarrow (W)$</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>Z</td>
</tr>
<tr>
<td>Description:</td>
<td>The contents of the W register are OR’ed with the 8-bit literal ‘k’. The result is placed in the W register.</td>
</tr>
</tbody>
</table>

### IORWF

**Inclusive OR W with f**

<table>
<thead>
<tr>
<th>Syntax:</th>
<th><code>[ label ] IORWF f,d</code></th>
</tr>
</thead>
</table>
| Operands: | $0 \leq f \leq 127$  
$ d \in \{0,1\}$ |
| Operation: | $(W) \ .OR. (f) \rightarrow \text{(destination)}$ |
| Status Affected: | Z |
| Description: | Inclusive OR the W register with register ‘f’. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’. |
**MOVF**

**Move f**

**Syntax:** `label MOVF f,d`

**Operands:**
- `0 ≤ f ≤ 127`
- `d ∈ [0,1]`

**Operation:** `(f) → (dest)`

**Status Affected:** `Z`

**Description:** The contents of register ‘f’ is moved to a destination dependent upon the status of ‘d’. If `d = 0`, destination is W register. If `d = 1`, the destination is file register ‘f’ itself. `d = 1` is useful to test a file register since Status flag Z is affected.

**Words:** 1

**Cycles:** 1

**Example:**

```
MOVF FSR, 0
```

**After Instruction**

- `W = value in FSR`
- `Z = 1`

---

**MOVF**

**Move W to f**

**Syntax:** `label MOVWF f`

**Operands:** `0 ≤ f ≤ 127`

**Operation:** `(W) → (f)`

**Status Affected:** None

**Description:** Move data from W register to register ‘f’.

**Words:** 1

**Cycles:** 1

**Example:**

```
MOVWF OPTION_REG, F
```

**Before Instruction**

- `OPTION_REG = 0xFF`
- `W = 0x4F`

**After Instruction**

- `OPTION_REG = 0x4F`
- `W = 0x4F`

---

**MOVLW**

**Move literal to W**

**Syntax:** `label MOVLW k`

**Operands:** `0 ≤ k ≤ 255`

**Operation:** `k → (W)`

**Status Affected:** None

**Description:** The 8-bit literal ‘k’ is loaded into W register. The “don’t cares” will assemble as ‘0’s.

**Words:** 1

**Cycles:** 1

**Example:**

```
MOVLW 0x5A
```

**After Instruction**

- `W = 0x5A`

---

**NOP**

**No Operation**

**Syntax:** `label NOP`

**Operands:** None

**Operation:** No operation

**Status Affected:** None

**Description:** No operation.

**Words:** 1

**Cycles:** 1

**Example:**

```
NOP
```
### RETFIE Return from Interrupt

**Syntax:**  
[ *label* ] RETFIE

**Operands:** None

**Operation:**  
TOS → PC,  
1 → GIE

**Status Affected:** None

**Description:** Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INT-CON<7>). This is a 2-cycle instruction.

**Words:** 1

**Cycles:** 2

**Example:**

<table>
<thead>
<tr>
<th>Before Instruction</th>
<th>After Instruction</th>
</tr>
</thead>
<tbody>
<tr>
<td>W = 0x07</td>
<td>W = value of k8</td>
</tr>
</tbody>
</table>

### RETLW Return with literal in W

**Syntax:**  
[ *label* ] RETLW *k*

**Operands:** 0 ≤ *k* ≤ 255

**Operation:**  
*k* → (W);  
TOS → PC

**Status Affected:** None

**Description:** The W register is loaded with the 8-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a 2-cycle instruction.

**Words:** 1

**Cycles:** 2

**Example:**

<table>
<thead>
<tr>
<th>TABLE</th>
<th>DONE</th>
</tr>
</thead>
<tbody>
<tr>
<td>CALL TABLE;W contains ;table offset ;value</td>
<td>GOTO DONE</td>
</tr>
<tr>
<td>ADDWF PC ;W = offset</td>
<td>RETLW k1 ;Begin table</td>
</tr>
<tr>
<td>RETLW k2</td>
<td>RETLW kn ;End of table</td>
</tr>
</tbody>
</table>

### RETURN Return from Subroutine

**Syntax:**  
[ *label* ] RETURN

**Operands:** None

**Operation:** TOS → PC

**Status Affected:** None

**Description:** Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a 2-cycle instruction.
## RLF Rotate Left f through Carry

**Syntax:**  
\[ \text{label} \] RLF \ f,d

**Operands:**  
\( 0 \leq f \leq 127 \)  
\( d \in [0,1] \)

**Operation:**  
See description below

**Status Affected:**  
C

**Description:**  
The contents of register ‘f’ are rotated one bit to the left through the Carry flag. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’.

**Example:**  
RLF REG1,0

<table>
<thead>
<tr>
<th>Before Instruction</th>
<th>After Instruction</th>
</tr>
</thead>
<tbody>
<tr>
<td>REG1 = 1110 0110</td>
<td>REG1 = 1110 0110</td>
</tr>
<tr>
<td>C = 0</td>
<td>W = 1100 1100</td>
</tr>
<tr>
<td></td>
<td>C = 1</td>
</tr>
</tbody>
</table>

**Words:**  
1

**Cycles:**  
1

## RRF Rotate Right f through Carry

**Syntax:**  
\[ \text{label} \] RRF \ f,d

**Operands:**  
\( 0 \leq f \leq 127 \)  
\( d \in [0,1] \)

**Operation:**  
See description below

**Status Affected:**  
C

**Description:**  
The contents of register ‘f’ are rotated one bit to the right through the Carry flag. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’.

## SLEEP Enter Sleep mode

**Syntax:**  
\[ \text{label} \] SLEEP

**Operands:**  
None

**Operation:**  
00h → WDT,  
0 → WDT prescaler,  
1 → TO,  
0 → PD

**Status Affected:**  
TO, PD

**Description:**  
The power-down Status bit, PD is cleared. Time-out Status bit, TO is set. Watchdog Timer and its prescaler are cleared. The processor is put into Sleep mode with the oscillator stopped.

## SUBLW Subtract W from literal

**Syntax:**  
\[ \text{label} \] SUBLW \ k

**Operands:**  
\( 0 \leq k \leq 255 \)

**Operation:**  
\( k - (W) \rightarrow (W) \)

**Status Affected:**  
C, DC, Z

**Description:**  
The W register is subtracted (2’s complement method) from the 8-bit literal ‘k’. The result is placed in the W register.

<table>
<thead>
<tr>
<th>Result</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>C = 0</td>
<td>( W &gt; k )</td>
</tr>
<tr>
<td>C = 1</td>
<td>( W \leq k )</td>
</tr>
<tr>
<td>DC = 0</td>
<td>( W&lt;3:0&gt; &gt; k&lt;3:0&gt; )</td>
</tr>
<tr>
<td>DC = 1</td>
<td>( W&lt;3:0&gt; \leq k&lt;3:0&gt; )</td>
</tr>
</tbody>
</table>
**SUBWF**  
Subtract W from f  
Syntax:  
\[[\text{label}]\] SUBWF f,d  
Operands:  
0 ≤ f ≤ 127  
d ∈ [0,1]  
Operation:  
(f) - (W) → (destination)  
Status Affected:  
C, DC, Z  
Description:  
Subtract (2’s complement method) W register from register ‘f’. If ‘d’ is ‘0’, the result is stored in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’.  

| C = 0 | W > f  
| C = 1 | W ≤ f  
| DC = 0 | W<3:0> > f<3:0>  
| DC = 1 | W<3:0> ≤ f<3:0>  

**SWAPF**  
Swap Nibbles in f  
Syntax:  
\[[\text{label}]\] SWAPF f,d  
Operands:  
0 ≤ f ≤ 127  
d ∈ [0,1]  
Operation:  
(f<3:0>) → (destination<7:4>),  
(f<7:4>) → (destination<3:0>)  
Status Affected:  
None  
Description:  
The upper and lower nibbles of register ‘f’ are exchanged. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed in register ‘f’.  

**XORWF**  
Exclusive OR W with f  
Syntax:  
\[[\text{label}]\] XORWF f,d  
Operands:  
0 ≤ f ≤ 127  
d ∈ [0,1]  
Operation:  
(W) .XOR. (f) → (destination)  
Status Affected:  
Z  
Description:  
Exclusive OR the contents of the W register with register ‘f’. If ‘d’ is ‘0’, the result is stored in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’.  

**XORLW**  
Exclusive OR literal with W  
Syntax:  
\[[\text{label}]\] XORLW k  
Operands:  
0 ≤ k ≤ 255  
Operation:  
(W) .XOR. k → (W)  
Status Affected:  
Z  
Description:  
The contents of the W register are XOR’ed with the 8-bit literal ‘k’. The result is placed in the W register.
24.0 ELECTRICAL SPECIFICATIONS

24.1 Absolute Maximum Ratings

Ambient temperature under bias ...................................................................................................... -40°C to +125°C
Storage temperature ........................................................................................................................ -65°C to +150°C

Voltage on pins with respect to Vss
- on VDD pin
  PIC10F320/322 .........................................................................................................  -0.3V to +6.5V
  PIC10LF320/322 .......................................................................................................  -0.3V to +4.0V
- on MCLR pin ..........................................................................................................................  -0.3V to +9.0V
- on all other pins ............................................................................................................  -0.3V to (VDD + 0.3V)

Maximum current
- on Vss pin
  -40°C ≤ TA ≤ +85°C ..............................................................................................................  250 mA
  +85°C ≤ TA ≤ +125°C .........................................................................................................  85 mA
- on VDD pin
  -40°C ≤ TA ≤ +85°C ..............................................................................................................  250 mA
  +85°C ≤ TA ≤ +125°C .........................................................................................................  85 mA
- Sunk by any I/O pin ...........................................................................................................  50 mA
- Sourced by any I/O pin ........................................................................................................  50 mA

Clamp current, IK (VPIN < 0 or VPIN > VDD) ................................................................................................... ±20 mA

Total power dissipation ........................................................................................................... 800 mW

Note 1: Maximum current rating requires even load distribution across I/O pins. Maximum current rating may be limited by the device package power dissipation characterizations, see Section 24.4 “Thermal Considerations” to calculate device specifications.

2: Power dissipation is calculated as follows: PDIS = VDD x (IDD – Σ IOH) + Σ ((VDD – VOH) x IOH) + Σ (VOL x IOL).

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.
24.2 Standard Operating Conditions

The standard operating conditions for any device are defined as:
Operating Voltage: \( V_{\text{DDMIN}} \leq V_{\text{DD}} \leq V_{\text{DDMAX}} \)
Operating Temperature: \( TA_{\text{MIN}} \leq TA \leq TA_{\text{MAX}} \)

**VDD — Operating Supply Voltage\(^{(1)}\)**

<table>
<thead>
<tr>
<th>Device Type</th>
<th>VDDMIN (Fosc ≤ 16 MHz)</th>
<th>VDDMIN (16 MHz &lt; Fosc ≤ 20 MHz)</th>
<th>VDDMAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC10LF320/322</td>
<td>+1.8V</td>
<td>+2.5V</td>
<td>+3.6V</td>
</tr>
<tr>
<td>PIC10F320/322</td>
<td>+2.3V</td>
<td>+2.5V</td>
<td>+5.5V</td>
</tr>
</tbody>
</table>

**TA — Operating Ambient Temperature Range**

<table>
<thead>
<tr>
<th>Temperature Level</th>
<th>TA_MIN</th>
<th>TA_MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Industrial Temperature</td>
<td>-40°C</td>
<td>+85°C</td>
</tr>
<tr>
<td>Extended Temperature</td>
<td>-40°C</td>
<td>+125°C</td>
</tr>
</tbody>
</table>

**Note 1:** See Parameter D001, DC Characteristics: Supply Voltage.
FIGURE 24-1: PIC10F320/322 VOLTAGE FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.
2: Refer to Table 24-6 for each Oscillator mode’s supported frequencies.

FIGURE 24-2: PIC10LF320/322 VOLTAGE FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.
2: Refer to Table 24-6 for each Oscillator mode’s supported frequencies.
### 24.3 DC Characteristics

<table>
<thead>
<tr>
<th>TABLE 24-1: SUPPLY VOLTAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Param. No.</strong></td>
</tr>
<tr>
<td>D001</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>D002*</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>VPOR*</td>
</tr>
<tr>
<td>VPORR*</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>D003</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>D004*</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 3.3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.
FIGURE 24-3: POR AND POR REARM WITH SLOW RISING VDD

Note 1: When NPOR is low, the device is held in Reset.
2: TPOR 1 μs typical.
3: TVLOW 2.7 μs typical.
## TABLE 24-2: SUPPLY VOLTAGE (IDD)\(^{(1,2)}\)

<table>
<thead>
<tr>
<th>Device Characteristics</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PIC10LF320/322</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>PIC10F320/322</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Param No.</strong></td>
<td><strong>Min.</strong></td>
<td><strong>Typ†</strong></td>
<td><strong>Max.</strong></td>
<td><strong>Units</strong></td>
<td><strong>Conditions</strong></td>
</tr>
<tr>
<td><strong>D013</strong></td>
<td>—</td>
<td>34</td>
<td>45</td>
<td>µA</td>
<td>1.8</td>
</tr>
<tr>
<td></td>
<td>—</td>
<td>60</td>
<td>105</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td>—</td>
<td>76</td>
<td>101</td>
<td>µA</td>
<td>2.3</td>
</tr>
<tr>
<td></td>
<td>—</td>
<td>110</td>
<td>148</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td>—</td>
<td>153</td>
<td>211</td>
<td>µA</td>
<td>5.0</td>
</tr>
<tr>
<td><strong>D013</strong></td>
<td>—</td>
<td>190</td>
<td>290</td>
<td>µA</td>
<td>1.8</td>
</tr>
<tr>
<td></td>
<td>—</td>
<td>350</td>
<td>500</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td><strong>D014</strong></td>
<td>—</td>
<td>290</td>
<td>430</td>
<td>µA</td>
<td>2.3</td>
</tr>
<tr>
<td></td>
<td>—</td>
<td>395</td>
<td>600</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td>—</td>
<td>480</td>
<td>775</td>
<td>µA</td>
<td>5.0</td>
</tr>
<tr>
<td><strong>D015</strong></td>
<td>—</td>
<td>0.8</td>
<td>1.3</td>
<td>mA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td>—</td>
<td>1.1</td>
<td>1.8</td>
<td>mA</td>
<td>3.6</td>
</tr>
<tr>
<td><strong>D015</strong></td>
<td>—</td>
<td>0.8</td>
<td>1.4</td>
<td>mA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td>—</td>
<td>1.1</td>
<td>1.8</td>
<td>mA</td>
<td>5.0</td>
</tr>
<tr>
<td><strong>D016</strong></td>
<td>—</td>
<td>2.2</td>
<td>4.1</td>
<td>µA</td>
<td>1.8</td>
</tr>
<tr>
<td></td>
<td>—</td>
<td>3.9</td>
<td>6.5</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td><strong>D016</strong></td>
<td>—</td>
<td>31</td>
<td>44</td>
<td>µA</td>
<td>2.3</td>
</tr>
<tr>
<td></td>
<td>—</td>
<td>40</td>
<td>57</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td><strong>D016A</strong></td>
<td>—</td>
<td>3.2</td>
<td>4.5</td>
<td>µA</td>
<td>1.8</td>
</tr>
<tr>
<td></td>
<td>—</td>
<td>4.8</td>
<td>7.0</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td><strong>D016A</strong></td>
<td>—</td>
<td>31</td>
<td>44</td>
<td>µA</td>
<td>2.3</td>
</tr>
<tr>
<td></td>
<td>—</td>
<td>40</td>
<td>57</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td>—</td>
<td>71</td>
<td>117</td>
<td>µA</td>
<td>5.0</td>
</tr>
</tbody>
</table>

**Note 1:** The test conditions for all IDD measurements in active operation mode are: CLKIN = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; MCLR = VDD; WDT disabled.

**Note 2:** The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.
### TABLE 24-2: SUPPLY VOLTAGE (I\text{DD})\textsuperscript{(1,2)} (CONTINUED)

<table>
<thead>
<tr>
<th>PIC10LF320/322</th>
<th>Standard Operating Conditions (unless otherwise stated)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Device Characteristics</strong></td>
<td><strong>Min.</strong></td>
</tr>
<tr>
<td>D017</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>—</td>
</tr>
<tr>
<td>D017</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>—</td>
</tr>
<tr>
<td>D018</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>—</td>
</tr>
<tr>
<td>D018</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>—</td>
</tr>
<tr>
<td>D019</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>—</td>
</tr>
<tr>
<td>D019</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>—</td>
</tr>
</tbody>
</table>

**Note 1:** The test conditions for all I\text{DD} measurements in active operation mode are: CLkin = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V\text{DD}; MCLR = V\text{DD}; WDT disabled.

**Note 2:** The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.
### TABLE 24-3: POWER-DOWN CURRENTS (I\text{PD})^{(1,2)}

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Device Characteristics</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max. +85°C</th>
<th>Max. +125°C</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>D023</td>
<td></td>
<td>—</td>
<td>0.06</td>
<td>1.1</td>
<td>2</td>
<td>µA</td>
<td>1.8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>0.08</td>
<td>1.3</td>
<td>2</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td>D023</td>
<td></td>
<td>—</td>
<td>0.20</td>
<td>1.1</td>
<td>2</td>
<td>µA</td>
<td>2.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>0.30</td>
<td>1.4</td>
<td>2</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>0.40</td>
<td>2.4</td>
<td>2.4</td>
<td>µA</td>
<td>5.0</td>
</tr>
<tr>
<td>D024</td>
<td></td>
<td>—</td>
<td>0.5</td>
<td>9</td>
<td>11</td>
<td>µA</td>
<td>1.8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>0.8</td>
<td>11</td>
<td>13</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td>D024</td>
<td></td>
<td>—</td>
<td>4.0</td>
<td>10</td>
<td>12</td>
<td>µA</td>
<td>2.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>4.2</td>
<td>12</td>
<td>14</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>4.3</td>
<td>14</td>
<td>16</td>
<td>µA</td>
<td>5.0</td>
</tr>
<tr>
<td>D025</td>
<td></td>
<td>—</td>
<td>30</td>
<td>96</td>
<td>120</td>
<td>µA</td>
<td>1.8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>39</td>
<td>106</td>
<td>123</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td>D025</td>
<td></td>
<td>—</td>
<td>32</td>
<td>96</td>
<td>120</td>
<td>µA</td>
<td>2.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>39</td>
<td>106</td>
<td>133</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>70</td>
<td>136</td>
<td>170</td>
<td>µA</td>
<td>5.0</td>
</tr>
<tr>
<td>D026</td>
<td></td>
<td>—</td>
<td>7.5</td>
<td>16</td>
<td>18</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>8</td>
<td>18</td>
<td>20</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td>D026</td>
<td></td>
<td>—</td>
<td>9</td>
<td>20</td>
<td>20.2</td>
<td>µA</td>
<td>5.0</td>
</tr>
<tr>
<td>D026A</td>
<td></td>
<td>—</td>
<td>2.7</td>
<td>10</td>
<td>15</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>3.0</td>
<td>10</td>
<td>15</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td>D026A</td>
<td></td>
<td>—</td>
<td>3.2</td>
<td>15</td>
<td>20</td>
<td>µA</td>
<td>5.0</td>
</tr>
<tr>
<td>D028</td>
<td></td>
<td>—</td>
<td>0.1</td>
<td>4</td>
<td>5</td>
<td>µA</td>
<td>1.8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>0.1</td>
<td>5</td>
<td>6</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td>D028</td>
<td></td>
<td>—</td>
<td>3.4</td>
<td>6</td>
<td>7</td>
<td>µA</td>
<td>2.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>3.6</td>
<td>7</td>
<td>8</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>3.8</td>
<td>8</td>
<td>9</td>
<td>µA</td>
<td>5.0</td>
</tr>
<tr>
<td>D029</td>
<td></td>
<td>—</td>
<td>250</td>
<td>—</td>
<td>—</td>
<td>µA</td>
<td>1.8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>250</td>
<td>—</td>
<td>—</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td>D029</td>
<td></td>
<td>—</td>
<td>280</td>
<td>—</td>
<td>—</td>
<td>µA</td>
<td>2.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>280</td>
<td>—</td>
<td>—</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>280</td>
<td>—</td>
<td>—</td>
<td>µA</td>
<td>5.0</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** The peripheral current is the sum of the base I\text{DD} or I\text{PD} and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base I\text{DD} or I\text{PD} current from this limit. Max values should be used when calculating total current consumption.

**Note 2:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V\text{DD}.

**Note 3:** A/D oscillator source is F\text{RC}.
## TABLE 24-4: I/O PORTS

### Standard Operating Conditions (unless otherwise stated)

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>D032</td>
<td>VIL</td>
<td>Input Low Voltage</td>
<td>—</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>I/O PORT:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>with TTL buffer</td>
<td>—</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
<td>4.5V ≤ VDD ≤ 5.5V</td>
</tr>
<tr>
<td>D032A</td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
<td>0.15</td>
<td>V</td>
<td>1.6V ≤ VDD ≤ 4.5V</td>
</tr>
<tr>
<td>D033</td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
<td>0.2</td>
<td>V</td>
<td>2.0V ≤ VDD ≤ 5.5V</td>
</tr>
<tr>
<td>D034</td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
<td>0.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>D040</td>
<td>VIH</td>
<td>Input High Voltage</td>
<td>2.0</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>4.5V ≤ VDD ≤ 5.5V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I/O ports:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>with TTL buffer</td>
<td>0.25</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>1.8V ≤ VDD ≤ 4.5V</td>
</tr>
<tr>
<td>D041</td>
<td></td>
<td></td>
<td>0.8</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>2.0V ≤ VDD ≤ 5.5V</td>
</tr>
<tr>
<td>D042</td>
<td></td>
<td></td>
<td>0.8</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>D060</td>
<td>IIL</td>
<td>Input Leakage Current(2)</td>
<td>—</td>
<td>± 5</td>
<td>± 125</td>
<td>nA</td>
<td>VSS ≤ VPIN ≤ VDD, Pin at high-impedance @ 85°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I/O ports</td>
<td>—</td>
<td>± 5</td>
<td>± 100</td>
<td>nA</td>
<td>125°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MCLR</td>
<td>—</td>
<td>± 5</td>
<td>± 200</td>
<td>nA</td>
<td>VSS ≤ VPIN ≤ VDD @ 85°C</td>
</tr>
<tr>
<td>D061</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D070*</td>
<td>IPUR</td>
<td>Weak Pull-up Current</td>
<td>25</td>
<td>100</td>
<td>200</td>
<td>µA</td>
<td>VDD = 3.3V, VPIN = VSS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>25</td>
<td>140</td>
<td>300</td>
<td>µA</td>
<td>VDD = 5.0V, VPIN = VSS</td>
</tr>
<tr>
<td>D080</td>
<td>VOL</td>
<td>Output Low Voltage</td>
<td>—</td>
<td>—</td>
<td>0.6</td>
<td>V</td>
<td>IOL = 8mA, VDD = 5V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I/O ports</td>
<td>—</td>
<td>—</td>
<td>0.6</td>
<td>V</td>
<td>IOL = 6mA, VDD = 3.3V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MCLR</td>
<td>—</td>
<td>—</td>
<td>0.6</td>
<td>V</td>
<td>IOL = 1.8mA, VDD = 1.8V</td>
</tr>
<tr>
<td>D090</td>
<td>VOH</td>
<td>Output High Voltage</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>IOH = 3.5mA, VDD = 5V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I/O ports</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>IOH = 3mA, VDD = 3.3V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MCLR</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>IOH = 1mA, VDD = 1.8V</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Negative current is defined as current sourced by the pin.

**Note 2:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
### TABLE 24-5: MEMORY PROGRAMMING REQUIREMENTS

**Standard Operating Conditions** (unless otherwise stated)

<table>
<thead>
<tr>
<th>Param No</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>D110</td>
<td>VHH</td>
<td>Program Memory Programming Specifications</td>
<td>8.0</td>
<td>—</td>
<td>9.0</td>
<td>V</td>
<td>(Note 2)</td>
</tr>
<tr>
<td>D111</td>
<td>IDD</td>
<td>Voltage on MCLR/VPP pin</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>D112</td>
<td>VDD</td>
<td>Supply Current during Programming</td>
<td>2.7</td>
<td>—</td>
<td>Vpp</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>D113</td>
<td>VPEW</td>
<td>VDD for Write or Row Erase</td>
<td>Vpp</td>
<td>—</td>
<td>Vpp</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>D114</td>
<td>IPPGM</td>
<td>Current on MCLR/VPP during Erase/Write</td>
<td>—</td>
<td>—</td>
<td>1.0</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>D115</td>
<td>IDD</td>
<td>Current on VDD during Erase/Write</td>
<td>—</td>
<td>—</td>
<td>5.0</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>D121</td>
<td>EP</td>
<td>Program Flash Memory</td>
<td>10K</td>
<td>—</td>
<td>—</td>
<td>E/W</td>
<td>-40°C to +85°C (Note 1)</td>
</tr>
<tr>
<td>D122</td>
<td>VPR</td>
<td>Cell Endurance</td>
<td>Vpp</td>
<td>—</td>
<td>Vpp</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>D123</td>
<td>TW</td>
<td>Self-timed Write Cycle Time</td>
<td>—</td>
<td>2</td>
<td>2.5</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>D124</td>
<td>TRET</td>
<td>Characteristic Retention</td>
<td>40</td>
<td>—</td>
<td>—</td>
<td>Year</td>
<td>Provided no other specifications are violated 0°C ≤ Ta ≤ 60, lower byte last 128 addresses</td>
</tr>
<tr>
<td>D125</td>
<td>EHEFC</td>
<td>High-Endurance Flash Cell</td>
<td>100K</td>
<td>—</td>
<td>—</td>
<td>E/W</td>
<td></td>
</tr>
</tbody>
</table>

† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Self-write and Block Erase.
**Note 2:** Required only if single-supply programming is disabled.
## 24.4 Thermal Considerations

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Typ.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>TH01</td>
<td>θJA</td>
<td>Thermal Resistance Junction to Ambient</td>
<td>60</td>
<td>°C/W</td>
<td>6-pin SOT-23 package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>80</td>
<td>°C/W</td>
<td>8-pin PDIP package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>90</td>
<td>°C/W</td>
<td>8-pin DFN package</td>
</tr>
<tr>
<td>TH02</td>
<td>θJC</td>
<td>Thermal Resistance Junction to Case</td>
<td>31.4</td>
<td>°C/W</td>
<td>6-pin SOT-23 package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>24</td>
<td>°C/W</td>
<td>8-pin PDIP package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>24</td>
<td>°C/W</td>
<td>8-pin DFN package</td>
</tr>
<tr>
<td>TH03</td>
<td>TJMAX</td>
<td>Maximum Junction Temperature</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>TH04</td>
<td>PD</td>
<td>Power Dissipation</td>
<td>—</td>
<td>W</td>
<td>PD = PINTERNAL + PI/O</td>
</tr>
<tr>
<td>TH05</td>
<td>PINTERNAL</td>
<td>Internal Power Dissipation</td>
<td>—</td>
<td>W</td>
<td>PINTERNAL = IDD x VDD</td>
</tr>
<tr>
<td>TH06</td>
<td>PI/O</td>
<td>I/O Power Dissipation</td>
<td>—</td>
<td>W</td>
<td>PVO = Σ (IOL * VOL) + Σ (IOH * (VDD - VOH))</td>
</tr>
<tr>
<td>TH07</td>
<td>PDER</td>
<td>Derated Power</td>
<td>—</td>
<td>W</td>
<td>PDER = PDMAX (TJ - TA)/θJA</td>
</tr>
</tbody>
</table>

**Note 1:**  
1. IDD is current to run the chip alone without driving any load on the output pins.  
2. TA = Ambient Temperature  
3. TJ = Junction Temperature
24.5 AC Characteristics

Timing Parameter Symbology has been created with one of the following formats:

1. TppS2ppS
2. TppS

<table>
<thead>
<tr>
<th>T</th>
<th>Frequency</th>
<th>T</th>
<th>Time</th>
</tr>
</thead>
</table>

Lowercase letters (pp) and their meanings:

<table>
<thead>
<tr>
<th>pp</th>
<th></th>
<th>pp</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>cc</td>
<td>CCP1</td>
<td>osc</td>
<td>CLKin</td>
</tr>
<tr>
<td>ck</td>
<td>CLKR</td>
<td>rd</td>
<td>RD</td>
</tr>
<tr>
<td>cs</td>
<td>CS</td>
<td>rw</td>
<td>RD or WR</td>
</tr>
<tr>
<td>di</td>
<td>SDI</td>
<td>sc</td>
<td>SCK</td>
</tr>
<tr>
<td>do</td>
<td>SDO</td>
<td>ss</td>
<td>SS</td>
</tr>
<tr>
<td>dt</td>
<td>Data in</td>
<td>t0</td>
<td>T0CKI</td>
</tr>
<tr>
<td>io</td>
<td>I/O PORT</td>
<td>t1</td>
<td>T1CKI</td>
</tr>
<tr>
<td>mc</td>
<td>MCLR</td>
<td>wr</td>
<td>WR</td>
</tr>
</tbody>
</table>

Uppercase letters and their meanings:

<table>
<thead>
<tr>
<th>S</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>F</td>
<td>Fall</td>
</tr>
<tr>
<td>H</td>
<td>High</td>
</tr>
<tr>
<td>I</td>
<td>Invalid (High-impedance)</td>
</tr>
<tr>
<td>L</td>
<td>Low</td>
</tr>
<tr>
<td>P</td>
<td>Period</td>
</tr>
<tr>
<td>R</td>
<td>Rise</td>
</tr>
<tr>
<td>V</td>
<td>Valid</td>
</tr>
<tr>
<td>Z</td>
<td>High-impedance</td>
</tr>
</tbody>
</table>

**FIGURE 24-4: LOAD CONDITIONS**

Load Condition

Pin

CL

VSS

Legend: CL=50 pF for all pins
FIGURE 24-5: CLOCK TIMING

TABLE 24-6: CLOCK OSCILLATOR TIMING REQUIREMENTS

<table>
<thead>
<tr>
<th>Standard Operating Conditions (unless otherwise stated)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Param No.</td>
</tr>
<tr>
<td>------------</td>
</tr>
<tr>
<td>OS01</td>
</tr>
<tr>
<td>OS02</td>
</tr>
<tr>
<td>OS03</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min” values with an external clock applied to CLKin pin. When an external clock input is used, the “max” cycle time limit is “DC” (no clock) for all devices.

TABLE 24-7: OSCILLATOR PARAMETERS

<table>
<thead>
<tr>
<th>Standard Operating Conditions (unless otherwise stated)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Param No.</td>
</tr>
<tr>
<td>------------</td>
</tr>
<tr>
<td>OS08</td>
</tr>
<tr>
<td>OS09</td>
</tr>
<tr>
<td>OS10*</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.
FIGURE 24-6: HFINTOSC FREQUENCY ACCURACY OVER DEVICE VDD AND TEMPERATURE

Temperature (°C) vs. VDD (V) graph showing frequency accuracy ranges:
-8% to +4%
±3%

VDD (V) range: 1.8 to 5.5
Temperature range: -40°C to 125°C
FIGURE 24-7: CLKR AND I/O TIMING

TABLE 24-8: CLKR AND I/O TIMING PARAMETERS

<table>
<thead>
<tr>
<th>Param. No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS11</td>
<td>TosH2ckL</td>
<td>Fosc↑ to CLKOUT↓(1)</td>
<td>—</td>
<td>—</td>
<td>70</td>
<td>ns</td>
<td>3.3V ≤ VDD ≤ 5.0V</td>
</tr>
<tr>
<td>OS12</td>
<td>TosH2ckH</td>
<td>Fosc↑ to CLKOUT↑(1)</td>
<td>—</td>
<td>—</td>
<td>72</td>
<td>ns</td>
<td>3.3V ≤ VDD ≤ 5.0V</td>
</tr>
<tr>
<td>OS13</td>
<td>TckL2ioV</td>
<td>CLKOUT↓ to Port out valid(1)</td>
<td>—</td>
<td>—</td>
<td>20</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>OS14</td>
<td>TioV2ckH</td>
<td>Port input valid before CLKOUT↑(1)</td>
<td>Tosc + 200 ns</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>OS15</td>
<td>TosH2ioV</td>
<td>Fosc↑ (Q1 cycle) to Port out valid</td>
<td>—</td>
<td>50</td>
<td>70*</td>
<td>ns</td>
<td>3.3V ≤ VDD ≤ 5.0V</td>
</tr>
<tr>
<td>OS16</td>
<td>TosH2ioI</td>
<td>Fosc↑ (Q2 cycle) to Port input invalid (I/O in setup time)</td>
<td>50</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>3.3V ≤ VDD ≤ 5.0V</td>
</tr>
<tr>
<td>OS17</td>
<td>TioV2osh</td>
<td>Port input valid to Fosc↑ (Q2 cycle) (I/O in setup time)</td>
<td>20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>OS18*</td>
<td>TioR</td>
<td>Port output rise time</td>
<td>—</td>
<td>40</td>
<td>72</td>
<td>ns</td>
<td>VDD = 1.8V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>15</td>
<td>32</td>
<td>ns</td>
<td>3.3V ≤ VDD ≤ 5.0V</td>
</tr>
<tr>
<td>OS19*</td>
<td>TioF</td>
<td>Port output fall time</td>
<td>—</td>
<td>28</td>
<td>55</td>
<td>ns</td>
<td>VDD = 1.8V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>15</td>
<td>30</td>
<td>ns</td>
<td>3.3V ≤ VDD ≤ 5.0V</td>
</tr>
<tr>
<td>OS20*</td>
<td>Tinp</td>
<td>INT pin input high or low time</td>
<td>25</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>OS21*</td>
<td>Tioc</td>
<td>Interrupt-on-change new input level time</td>
<td>25</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated.

Note 1: Measurements are taken in EXTRC mode where CLKOUT output is 4 x Tosc.
FIGURE 24-8:  RESET, WATCHDOG TIMER, AND POWER-UP TIMER TIMING

Note 1: Asserted low.

FIGURE 24-9:  BROWN-OUT RESET TIMING AND CHARACTERISTICS
TABLE 24-9: RESET, WATCHDOG TIMER, POWER-UP TIMER AND BROWN-OUT RESET PARAMETERS

Standard Operating Conditions (unless otherwise stated)

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>TMCL</td>
<td>MCLR Pulse Width (low)</td>
<td>2</td>
<td>—</td>
<td>—</td>
<td>µs</td>
<td>VDD = 3.3-5V, -40°C to +85°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>5</td>
<td>—</td>
<td>—</td>
<td>µs</td>
<td>VDD = 3.3-5V</td>
</tr>
<tr>
<td>31</td>
<td>TWDTLP</td>
<td>Low-Power Watchdog Timer Time-out Period</td>
<td>10</td>
<td>16</td>
<td>27</td>
<td>ms</td>
<td>VDD = 3.3V-5V 1:16 Prescaler used</td>
</tr>
<tr>
<td>33*</td>
<td>TPWRT</td>
<td>Power-up Timer Period, PWRTE = 0</td>
<td>40</td>
<td>64</td>
<td>140</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>34*</td>
<td>TIOZ</td>
<td>I/O high-impedance from MCLR Low or Watchdog Timer Reset</td>
<td>—</td>
<td>—</td>
<td>2.0</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>35</td>
<td>VBOR</td>
<td>Brown-out Reset Voltage(1)</td>
<td>2.55</td>
<td>2.70</td>
<td>2.85</td>
<td>V</td>
<td>BORV = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.30</td>
<td>2.40</td>
<td>2.55</td>
<td>V</td>
<td>BORV = 1 (PIC10F320/322)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.80</td>
<td>1.90</td>
<td>2.05</td>
<td>V</td>
<td>BORV = 1 (PIC10LF320/322)</td>
</tr>
<tr>
<td>36*</td>
<td>VHYST</td>
<td>Brown-out Reset Hysteresis</td>
<td>0</td>
<td>25</td>
<td>50</td>
<td>mV</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>37*</td>
<td>T0RDC</td>
<td>Brown-out Reset DC Response Time</td>
<td>1</td>
<td>3</td>
<td>5</td>
<td>µs</td>
<td>VDD ≤ VBOR</td>
</tr>
<tr>
<td>38</td>
<td>VLPBOR</td>
<td>Low-Power Brown-Out Reset Voltage</td>
<td>1.8</td>
<td>2.1</td>
<td>2.5</td>
<td>V</td>
<td>LPBOR = 1</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.  
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested. 

Note 1: To ensure these voltage tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

FIGURE 24-10: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

![Timer0 and Timer1 External Clock Timings Diagram]

TABLE 24-10: TIMER0 EXTERNAL CLOCK REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>40*</td>
<td>T0H</td>
<td>TOCKI High Pulse Width</td>
<td>No Prescaler</td>
<td>0.5 TCY + 20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>With Prescaler</td>
<td>10</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>41*</td>
<td>T0L</td>
<td>TOCKI Low Pulse Width</td>
<td>No Prescaler</td>
<td>0.5 TCY + 20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>With Prescaler</td>
<td>10</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>42*</td>
<td>T0P</td>
<td>TOCKI Period</td>
<td>Greater of: 20 or TCY + 40 N</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>N = prescale value (2, 4, ..., 256)</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.  
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
TABLE 24-11: CONFIGURATION LOGIC CELL (CLC) CHARACTERISTICS

<table>
<thead>
<tr>
<th>Param. No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLC01*</td>
<td>T CLCIN</td>
<td>CLC input time</td>
<td>—</td>
<td>7</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>CLC02*</td>
<td>T CLC</td>
<td>CLC module input to output propagation time</td>
<td>—</td>
<td>24</td>
<td>—</td>
<td>ns</td>
<td>VDD = 1.8V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>VDD &gt; 3.6V</td>
</tr>
<tr>
<td>CLC03*</td>
<td>T CLCOUT</td>
<td>CLC output time</td>
<td>—</td>
<td>OS18</td>
<td>—</td>
<td>—</td>
<td>(Note 1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Rise Time</td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fall Time</td>
<td>—</td>
<td>OS19</td>
<td>—</td>
<td>—</td>
<td>(Note 1)</td>
</tr>
<tr>
<td>CLC04*</td>
<td>F CLCMAX</td>
<td>CLC maximum switching frequency</td>
<td>—</td>
<td>45</td>
<td>—</td>
<td>MHz</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: See FIGURE 19-1: CLCx Simplified Block Diagram, to identify specific CLC signals.

Note 1: See Table 24-8 for OS18 and OS19 rise and fall times.
TABLE 24-12: A/D CONVERTER (ADC) CHARACTERISTICS:

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD01</td>
<td>NR</td>
<td>Resolution</td>
<td>—</td>
<td>—</td>
<td>8</td>
<td>bit</td>
<td></td>
</tr>
<tr>
<td>AD02</td>
<td>EIL</td>
<td>Integral Error</td>
<td>—</td>
<td>—</td>
<td>±1.7</td>
<td>LSb</td>
<td>VREF = 3.0V</td>
</tr>
<tr>
<td>AD03</td>
<td>EDL</td>
<td>Differential Error</td>
<td>—</td>
<td>—</td>
<td>±1</td>
<td>LSb</td>
<td>No missing codes</td>
</tr>
<tr>
<td>AD04</td>
<td>EOFF</td>
<td>Offset Error</td>
<td>—</td>
<td>—</td>
<td>±2.5</td>
<td>LSb</td>
<td>VREF = 3.0V</td>
</tr>
<tr>
<td>AD05</td>
<td>EGN</td>
<td>Gain Error</td>
<td>—</td>
<td>—</td>
<td>±2.0</td>
<td>LSb</td>
<td>VREF = 3.0V</td>
</tr>
<tr>
<td>AD06</td>
<td>VREF</td>
<td>Reference Voltage</td>
<td>1.8</td>
<td>—</td>
<td>VDD</td>
<td>V</td>
<td>VREF = (VREF+ minus VREF-)</td>
</tr>
<tr>
<td>AD07</td>
<td>VAIN</td>
<td>Full-Scale Range</td>
<td>VSS</td>
<td>—</td>
<td>VREF</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>AD08</td>
<td>ZAIN</td>
<td>Recommended Impedance of</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>kΩ</td>
<td>Can go higher if external 0.01μF capacitor is present on input pin.</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Total Absolute Error includes integral, differential, offset and gain errors.
2: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.
3: When ADC is off, it will not consume any current other than leakage current. The power-down current specification includes any such leakage from the ADC module.

TABLE 24-13: A/D CONVERSION REQUIREMENTS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD130*</td>
<td>TAD</td>
<td>A/D Clock Period</td>
<td>1.0</td>
<td>—</td>
<td>6.0</td>
<td>μs</td>
<td>Tosc-based</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A/D Internal FRC Oscillator Period</td>
<td>1.0</td>
<td>1.6</td>
<td>6.0</td>
<td>μs</td>
<td>ADCS&lt;1:0&gt; = 11 (ADRC mode)</td>
</tr>
<tr>
<td>AD131</td>
<td>TCNV</td>
<td>Conversion Time (not including Acquisition Time)†(1)</td>
<td>—</td>
<td>9.5</td>
<td>—</td>
<td>TAD</td>
<td>Set GO/DONE bit to conversion complete</td>
</tr>
<tr>
<td>AD132*</td>
<td>TACQ</td>
<td>Acquisition Time</td>
<td>—</td>
<td>5.0</td>
<td>—</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>AD133*</td>
<td>THCD</td>
<td>Holding Capacitor Disconnect Time</td>
<td>—</td>
<td>1/2 TAD</td>
<td>—</td>
<td>Fosc-based</td>
<td>ADCS&lt;2:0&gt; = x11 (ADC FRC mode)</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The ADRES register may be read on the following TCY cycle.
FIGURE 24-12: A/D CONVERSION TIMING (NORMAL MODE)

Note 1: If the A/D clock source is selected as FRC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

FIGURE 24-13: A/D CONVERSION TIMING (SLEEP MODE)

Note 1: If the A/D clock source is selected as FRC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.
25.0 DC AND AC CHARACTERISTICS GRAPHS AND CHARTS

Graphs and charts are not available at this time.
26.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICkit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

26.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:
- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:
- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:
- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:
- Local file history feature
- Built-in support for Bugzilla issue tracker
26.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip’s 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

26.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

26.4 MPLINK Object Linker/
MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

26.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility
26.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

26.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip’s next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer’s PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

26.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip’s most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer’s PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

26.9 PICkit 3 In-Circuit Debugger/Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer’s PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

26.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.
26.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, Keeloq® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

26.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

• Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
• Software Tools from companies, such as Gimpel and Trace Systems
• Protocol Analyzers from companies, such as Saleae and Total Phase
• Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
• Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®
27.0 PACKAGING INFORMATION

27.1 Package Marking Information

Legend:
- XX...X Product-specific information
- Y Year code (last digit of calendar year)
- YY Year code (last 2 digits of calendar year)
- WW Week code (week of January 1 is week ‘01’)
- NNN Alphanumeric traceability code
- \( \text{Pb-free JEDEC® designator for Matte Tin (Sn)} \)
- * This package is Pb-free. The Pb-free JEDEC designator (\( \text{(e3)} \)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.
## TABLE 27-1: 8-LEAD 2x3 DFN (MC) TOP MARKING

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Marking</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC10F322(T)-I/MC</td>
<td>BAA</td>
</tr>
<tr>
<td>PIC10F322(T)-E/MC</td>
<td>BAB</td>
</tr>
<tr>
<td>PIC10F320(T)-I/MC</td>
<td>BAC</td>
</tr>
<tr>
<td>PIC10F320(T)-E/MC</td>
<td>BAD</td>
</tr>
<tr>
<td>PIC10LF322(T)-I/MC</td>
<td>BAF</td>
</tr>
<tr>
<td>PIC10LF322(T)-E/MC</td>
<td>BAG</td>
</tr>
<tr>
<td>PIC10LF320(T)-I/MC</td>
<td>BAH</td>
</tr>
<tr>
<td>PIC10LF320(T)-E/MC</td>
<td>BAJ</td>
</tr>
</tbody>
</table>

## TABLE 27-2: 6-LEAD SOT-23 (OT) PACKAGE TOP MARKING

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Marking</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC10F322(T)-I/OT</td>
<td>LA/LJ</td>
</tr>
<tr>
<td>PIC10F322(T)-E/OT</td>
<td>LB/LK</td>
</tr>
<tr>
<td>PIC10F320(T)-I/OT</td>
<td>LC</td>
</tr>
<tr>
<td>PIC10F320(T)-E/OT</td>
<td>LD</td>
</tr>
<tr>
<td>PIC10LF322(T)-I/OT</td>
<td>LE</td>
</tr>
<tr>
<td>PIC10LF322(T)-E/OT</td>
<td>LF</td>
</tr>
<tr>
<td>PIC10LF320(T)-I/OT</td>
<td>LG</td>
</tr>
<tr>
<td>PIC10LF320(T)-E/OT</td>
<td>LH</td>
</tr>
</tbody>
</table>
27.2 Package Details
The following sections give the technical details of the packages.

6-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com-packaging

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Outside Lead Pitch</td>
<td>e1</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
</tr>
<tr>
<td>Footprint</td>
<td>L1</td>
</tr>
<tr>
<td>Foot Angle</td>
<td>φ</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
</tbody>
</table>

Notes:
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B
6-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com-packaging

---

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Contact Pitch</td>
<td>E</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C</td>
</tr>
<tr>
<td>Contact Pad Width (X6)</td>
<td>X</td>
</tr>
<tr>
<td>Contact Pad Length (X6)</td>
<td>Y</td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>G</td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>GX</td>
</tr>
<tr>
<td>Overall Width</td>
<td>Z</td>
</tr>
</tbody>
</table>

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028A
8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

Microchip Technology Drawing No. C04-018D Sheet 1 of 2
### 8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at [http://www.microchip.com/packaging](http://www.microchip.com/packaging)

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**Units**

<table>
<thead>
<tr>
<th>Dimension Limits</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Pins</td>
<td>N</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
<td>.100 BSC</td>
<td></td>
</tr>
<tr>
<td>Top to Seating Plane</td>
<td>A</td>
<td>-</td>
<td>.210</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
<td>.115</td>
<td>.130</td>
</tr>
<tr>
<td>Base to Seating Plane</td>
<td>A1</td>
<td>.015</td>
<td>-</td>
</tr>
<tr>
<td>Shoulder to Shoulder Width</td>
<td>E</td>
<td>.290</td>
<td>.310</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
<td>.240</td>
<td>.250</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
<td>.348</td>
<td>.365</td>
</tr>
<tr>
<td>Tip to Seating Plane</td>
<td>L</td>
<td>.115</td>
<td>.130</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
<td>.008</td>
<td>.010</td>
</tr>
<tr>
<td>Upper Lead Width</td>
<td>b1</td>
<td>.040</td>
<td>.060</td>
</tr>
<tr>
<td>Lower Lead Width</td>
<td>b</td>
<td>.014</td>
<td>.018</td>
</tr>
<tr>
<td>Overall Row Spacing</td>
<td>eB</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

---

**TOP VIEW**

**BOTTOM VIEW**

---

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N   8</td>
</tr>
<tr>
<td>Pitch</td>
<td>e   0.50 BSC</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A   0.80 0.90 1.00</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1  0.00 0.02 0.05</td>
</tr>
<tr>
<td>Contact Thickness</td>
<td>A3  0.20 REF</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D   2.00 BSC</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E   3.00 BSC</td>
</tr>
<tr>
<td>Exposed Pad Length</td>
<td>D2</td>
</tr>
<tr>
<td>Exposed Pad Width</td>
<td>E2</td>
</tr>
<tr>
<td>Contact Width</td>
<td>b   0.20 0.25 0.30</td>
</tr>
<tr>
<td>Contact Length</td>
<td>L   0.30 0.40 0.50</td>
</tr>
<tr>
<td>Contact-to-Exposed Pad</td>
<td>K</td>
</tr>
</tbody>
</table>

**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   - REF: Reference Dimension, usually without tolerance, for information purposes only.

---

Microchip Technology Drawing C04-123C
**PIC10(L)F320/322**

8-Lead Plastic Dual Flat, No Lead Package (MC) - 2x3x0.9mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

![Recommended Land Pattern Diagram]

**Recommended Land Pattern**

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Contact Pitch</td>
<td>E</td>
</tr>
<tr>
<td>Optional Center Pad Width</td>
<td>W2</td>
</tr>
<tr>
<td>Optional Center Pad Length</td>
<td>T2</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C1</td>
</tr>
<tr>
<td>Contact Pad Width (X8)</td>
<td>X1</td>
</tr>
<tr>
<td>Contact Pad Length (X8)</td>
<td>Y1</td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>G</td>
</tr>
</tbody>
</table>

**Notes:**
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2123B
APPENDIX A: DATA SHEET

REVISION HISTORY

Revision A (07/2011)
Original release.

Revision B (02/2014)
Electrical Specifications update and new formats;
Minor edits.

Revision C (05/2015)
Updated Figures 7-1 and 11-1. Update Sections 5.4.1,
24.1, and 24.3. Updated Tables 24-2 and 24-9.

Revision D (11/2015)
Updated the “eXtreme Low-Power (XLP) Features”
section; added “Memory” section. Updated “Family
Types” table; Updated Table 2-1, 24-5, 24-7, 24-9,
24-12 and 24-13; Updated Figure 7-1, 24-6 and section
15.2.5; Other minor corrections.
THE MICROCHIP WEBSITE

Microchip provides online support via our website at www.microchip.com. This website is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the website contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user’s guides and hardware support documents, latest software releases and archived software
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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<table>
<thead>
<tr>
<th>PART NO.</th>
<th>Device</th>
<th>Tape and Reel Option</th>
<th>Temperature Range</th>
<th>Package</th>
<th>Pattern</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>PIC10F320, PIC10LF320, PIC10F322, PIC10LF322</td>
<td>Blank = Standard packaging (tube or tray) T = Tape and Reel[1]</td>
<td>I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)</td>
<td>OT = SOT-23 P = PDIP MC = DFN</td>
<td>QTP, SQTP, Code or Special Requirements (blank otherwise)</td>
</tr>
</tbody>
</table>

Examples:

a) PIC10LF320T - I/OT Tape and Reel, Industrial temperature, SOT-23 package
b) PIC10F322 - I/P Industrial temperature PDIP package
c) PIC10F322 - E/MC Extended temperature, DFN package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
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