Si873x Data Sheet

Low Input Current LED Emulator, Logic Output Isolators

The Si873x isolators are pin-compatible, single-channel, drop-in replacements for popular optocouplers with data rates up to 15 Mbps. These devices isolate high-speed digital signals and offer performance, reliability, and flexibility advantages not available with optocoupler solutions. The Si873x series is based on Silicon Labs' proprietary CMOS isolation technology for low-power and high-speed operation and are resistant to the wear-out effects found in optocouplers that degrade performance with increasing temperature, forward current, and device age. As a result, the Si873x series offer longer service life and dramatically higher reliability compared to optocouplers. Ordering options include logic output with and without output enable options.

Applications

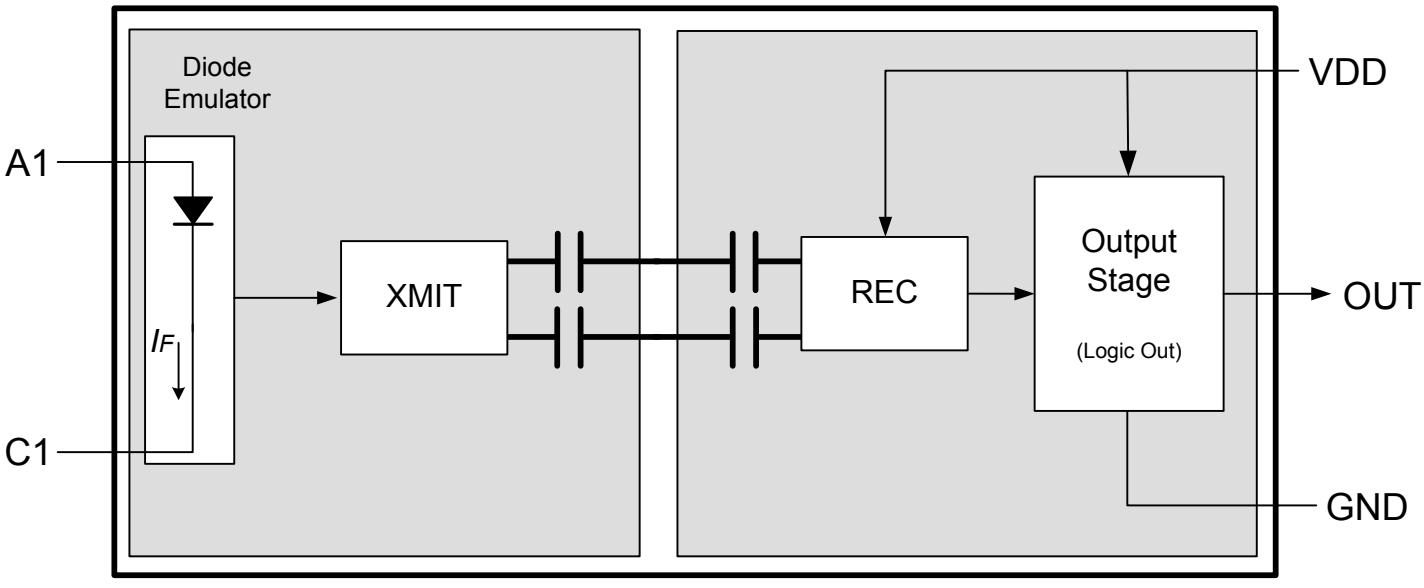
- Industrial automation systems
- Motor controls and drives
- Isolated switch mode power supplies
- Isolated data acquisition
- Test and measurement equipment

Safety Regulatory Approvals

- UL 1577 recognized
  - Up to 2500 V_{RMS} for 1 minute
- CSA component notice 5 A approval
- VDE certification conformity
  - VDE0884-10 (basic/reinforced insulation)
- CQC certification approval
  - GB4943.1

KEY FEATURES

- High Speed: dc to 15 Mbps
- 2.5 to 5.5 V logic output
- Pin-compatible, drop-in upgrades for popular high-speed digital optocouplers
- Performance and reliability advantages vs. optocouplers:
  - Resistant to temperature, age and forward current effects
  - 10x lower FIT rate for longer service life
  - Lower power and forward input diode current
- 1 channel diode emulator input
- Propagation delay 30 ns
- 10 kV surge withstand capability
- AEC-Q100 qualified
- Wide operating temperature range: – 40 to +125 °C
- RoHS-compliant packages: SOIC-8 (Narrow body)



1. Ordering Guide

Table 1.1. Si873x Ordering Guide[1, 2, 3, 4]

Ordering Part Number (OPN)	Ordering Options				
	Input/Output Configuration	Data Rate Cross Reference	Insulation Rating	Enable Pin/ Output State when Active	Package Type
Logic Output					
Si8735BC-IS	High CMTI Non-inverting Output	15 Mbps HCPL-0201	3.75 kVrms	No, N/A	SOIC-8
Si8736BC-IS	High CMTI Inverting Output	15 Mbps ACPL-061L, HCPL-0600, HCPL-0601, HCPL-0611	3.75 kVrms	Yes, High	SOIC-8

Note:

1. All packages are RoHS-compliant with peak solder reflow temperatures of 260 °C according to the JEDEC industry standard classifications.
2. “Si” and “SI” are used interchangeably.
3. AEC-Q100 qualified.
4. An “R” at the end of the part number denotes Tape and Reel packaging option.

Table of Contents

2. Application Information

2.1 Theory of Operation

The Si873x are pin-compatible, single-channel, drop-in replacements for popular optocouplers with data rates up to 15 Mbps. The operation of an Si873x channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for the Si873x is shown in the figure below.

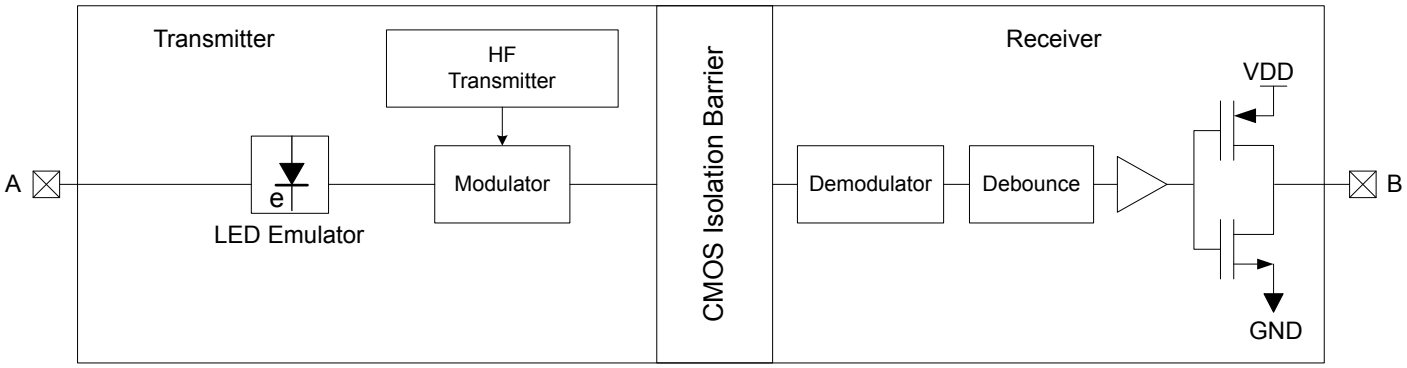


Figure 2.1. Simplified Channel Diagram

3. Functional Description

3.1 Device Behavior

Truth tables for the Si873x are summarized in the table below.

Table 3.1. Si873x Truth Table Summary

Input	Enable	Output
Si8735 (Non-inverting)		
OFF	N/A	LOW
ON	N/A	HIGH
Si8736 (Inverting)		
OFF	HIGH	HIGH
ON	HIGH	LOW
X	LOW	HIGH
Note: This truth table assumes VDD is powered (VDD> UVLO). If VDD is below UVLO, see 3.3 Under Voltage Lockout (UVLO) for more information. When VDD < UVLO, the output state is not guaranteed. In this condition, the output level is determined by external circuity connected to the output.		

3.2 Device Startup

During startup-up, for the Si873x, Output V_O is high until V_{DD} rises above the UVLO+ threshold for a minimum time period of t_{START}. Following this, the output is low when the current flowing from anode to cathode is > $I_{F(ON)}$. Device startup, normal operation, and shut-down behavior for the Si873x is shown in the figure below. Note that the figure below assumes that Enable is asserted and that the outputs are operating in their normal operating condition (inverting for the Si8736). See the table above for more details on the Enable function.

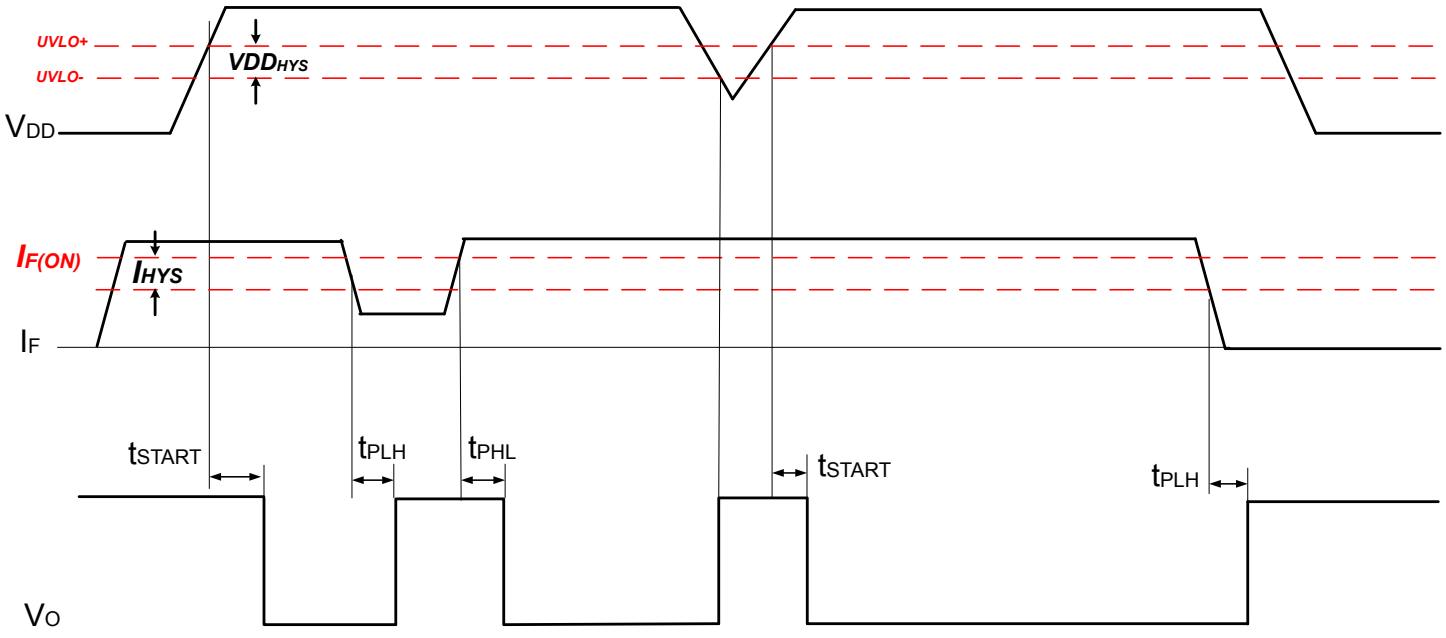


Figure 3.1. Si8736 Operating Behavior (I_F > $I_{F(MIN)}$ when V_F > $V_{F(MIN)}$)

3.3 Under Voltage Lockout (UVLO)

The UVLO circuit unconditionally drives V_O to its default state when V_{DD} is below the lockout threshold. Referring to the figure below, upon power up, the Si873x is maintained in UVLO until VDD rises above VDD_{UV+}. During power down, the Si873x enters UVLO when VDD falls below the UVLO threshold plus hysteresis (i.e., VDD < VDD_{UV+} – VDD_{HYS}).

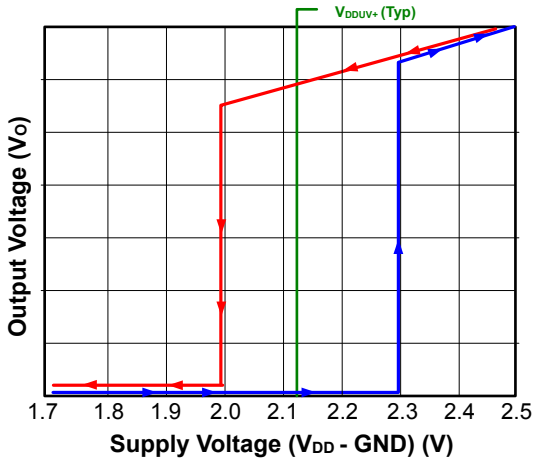


Figure 3.2. Si873x UVLO Response

4. Applications

The following sections detail the input and output circuits necessary for proper operation of the Si873x family.

4.1 Input Circuit Design

Opto coupler manufacturers typically recommend the circuits shown in the figures below. These circuits are specifically designed to improve opto-coupler input common-mode rejection and increase noise immunity.

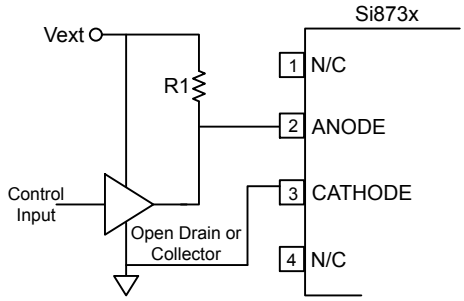


Figure 4.1. Si873x Input Circuit

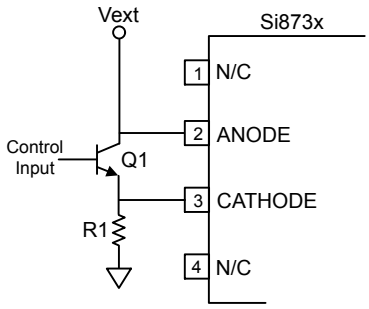


Figure 4.2. High CMR Si873x Input Circuit

The optically-coupled circuit of Figure 4.1 Si873x Input Circuit on page 7 turns the LED on when the control input is high. However, internal capacitive coupling from the LED to the power and ground conductors can momentarily force the LED into its off state when the anode and cathode inputs are subjected to a high common-mode transient. The circuit shown in Figure 4.2 High CMR Si873x Input Circuit on page 7 addresses this issue by using a value of R1 sufficiently low to overdrive the LED, ensuring it remains on during an input common-mode transient. Q1 shorts the LED off in the low output state, again increasing common-mode transient immunity.

Some opto coupler applications recommend reverse-biasing the LED when the control input is off to prevent coupled noise from energizing the LED. The Si873x input circuit requires less current and has twice the off-state noise margin compared to opto couplers. However, high CMR opto coupler designs that overdrive the LED (see Figure 4.2 High CMR Si873x Input Circuit on page 7) may require increasing the value of R1 to limit input current I_F to its maximum rating when using the Si873x. In addition, there is no benefit in driving the Si873x input diode into reverse bias when in the off state. Consequently, opto coupler circuits using this technique should either leave the negative bias circuitry unpopulated or modify the circuitry (e.g., add a clamp diode or current limiting resistor) to ensure that the anode pin of the Si873x is no more than –0.3 V with respect to the cathode when reverse-biased.

New designs should consider the input circuit configurations of Figure 4.3 Si873x Other Input Circuit Configurations on page 8, which are more efficient than those of the figures above. As shown, S1 and S2 represent any suitable switch, such as a BJT or MOSFET, analog transmission gate, processor I/O, etc. Also, note that the Si873x input can be driven from the I/O port of any MCU or FPGA capable of sourcing a minimum of 6 mA (see Figure 4.3 Si873x Other Input Circuit Configurations on page 8C). Additionally, note that the Si873x propagation delay and output drive do not significantly change for values of I_F between $I_{F(MIN)}$ and $I_{F(MAX)}$.

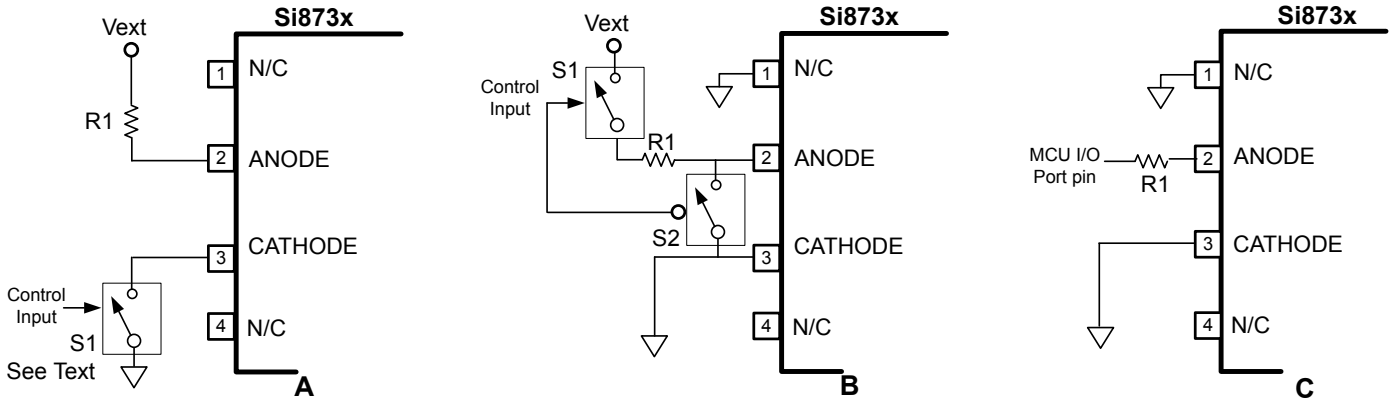


Figure 4.3. Si873x Other Input Circuit Configurations

4.2 Output Circuit Design and Power Supply Connections

GND can be biased at, above, or below ground as long as the voltage on V_{DD} with respect to GND is a maximum of 5.5 V. V_{DD} decoupling capacitors should be placed as close to the package pins as possible. The optimum values for these capacitors depend on load current and the distance between the chip and its power source. It is recommended that 0.1 and 1 µF bypass capacitors be used to reduce high-frequency noise and maximize performance. Opto replacement applications should limit their supply voltages to 5.5 V or less.

5. Electrical Specifications

Table 5.1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
V_{DD} Supply Voltage	V_{DD}	2.5	—	5.5	V
Input Current	$I_{F(ON)}$ (See Figure 5.1 Diode Emulator Model and I-V Curve on page 11)	1	2.2	15	mA
Operating Temperature (Ambient)	T_A	–40	—	125	°C

Table 5.2. Electrical Characteristics

V_{DD} =5 V; GND=0 V; T_A =–40 to +125 °C; typical specs at 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Parameters						
Supply Voltage	V_{DD}	(V_{DD}–GND)	2.5	—	5.5	V
Supply Current	I_{DD}	Output high or low (V_{DD} = 2.5 to 5.5 V)	—	1.5	—	mA
Input Current Threshold	$I_{F(TH)}$		—	0.68	—	mA
Input Current Hysteresis	I_{HYS}		—	0.18	—	mA
Input Forward Voltage (OFF)	$V_{F(OFF)}$	Measured at ANODE with respect to CATHODE.	—	—	1	V
Input Forward Voltage (ON)	$V_{F(ON)}$	Measured at ANODE with respect to CATHODE.	1.4	—	2.8	V
Input Capacitance	C_I	f = 100 kHz, V_F = 0 V, V_F = 2 V	— —	15 15	— —	pF pF
Logic Low Output Voltage	V_{OL}	I_{OL} = 4 mA	—	0.2	0.4	V
Logic High Output Voltage	V_{OH}	I_{OH} = –4 mA	V_{DD} - 0.4	V_{DD} - 0.2	—	V
Output Impedance	Z_O		—	50	—	Ω
Enable High Min	V_{EH}		V_{DD} - 0.4	—	—	V
Enable Low Max	V_{EL}		—	—	0.4	V
Enable High Current Draw	I_{EH}	V_{DD} = V_{EH} = 5 V	—	0	—	µA
Enable Low Current Draw	I_{EL}	V_{DD} = 5 V, V_{EL} = 0 V	—	–30	0	µA
UVLO Threshold +	VDD_{UV+}	See Figure 3.2 Si873x UVLO Response on page 6. V_{DD} rising	—	2.2	2.35	V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
UVLO Threshold –	VDD_{UV-}	See Figure 3.2 Si873x UVLO Response on page 6. V_{DD} falling	—	2	2.25	V
UVLO lockout hysteresis	VDD_{HYS}		50	100	—	mV
AC Switching Parameters (V_{DD} = 5 V, C_L = 15 pF)						
Maximum Data Rate	F_{DATA}		DC	—	15	M_{BPS}
Minimum Pulse Width	MPW		66	—	—	ns
Propagation Delay (Low-to-High)	t_{PLH}	C_L = 15 pF	5	—	50	ns
Propagation Delay (High-to-Low)	t_{PHL}	C_L = 15 pF	1.5	—	50	ns
Pulse Width Distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	—	—	25	ns
Propagation Delay Skew	$t_{PSK(p-p)}$	$t_{PSK(P-P)}$ is the magnitude of the difference in prop delays between different units operating at same supply voltage, load, and ambient temp.	—	—	25	ns
Rise Time*	t_R	C_L = 15 pF	—	2.5	4	ns
Fall Time*	t_F	C_L = 15 pF	—	2.5	4	ns
Device Startup Time	t_{START}		—	—	40	µs
Common Mode Transient Immunity	CMTI	Output = low or high V_{CM} = 1500 V (See Figure 5.2 Common Mode Transient Immunity Characterization Circuit on page 12) I_F = 2.2 mA	—	25	—	kV/µs

Note: Guaranteed by design and/or characterization

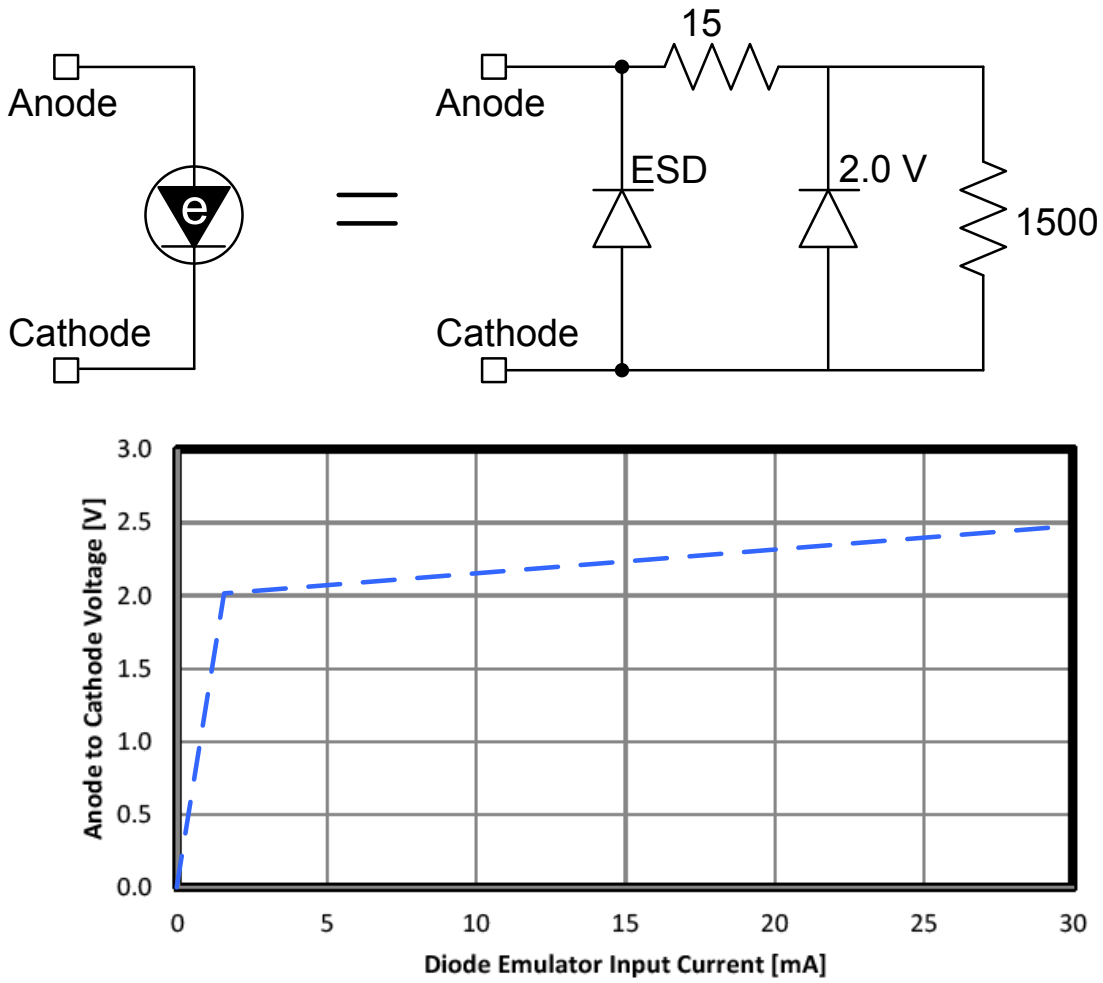


Figure 5.1. Diode Emulator Model and I-V Curve

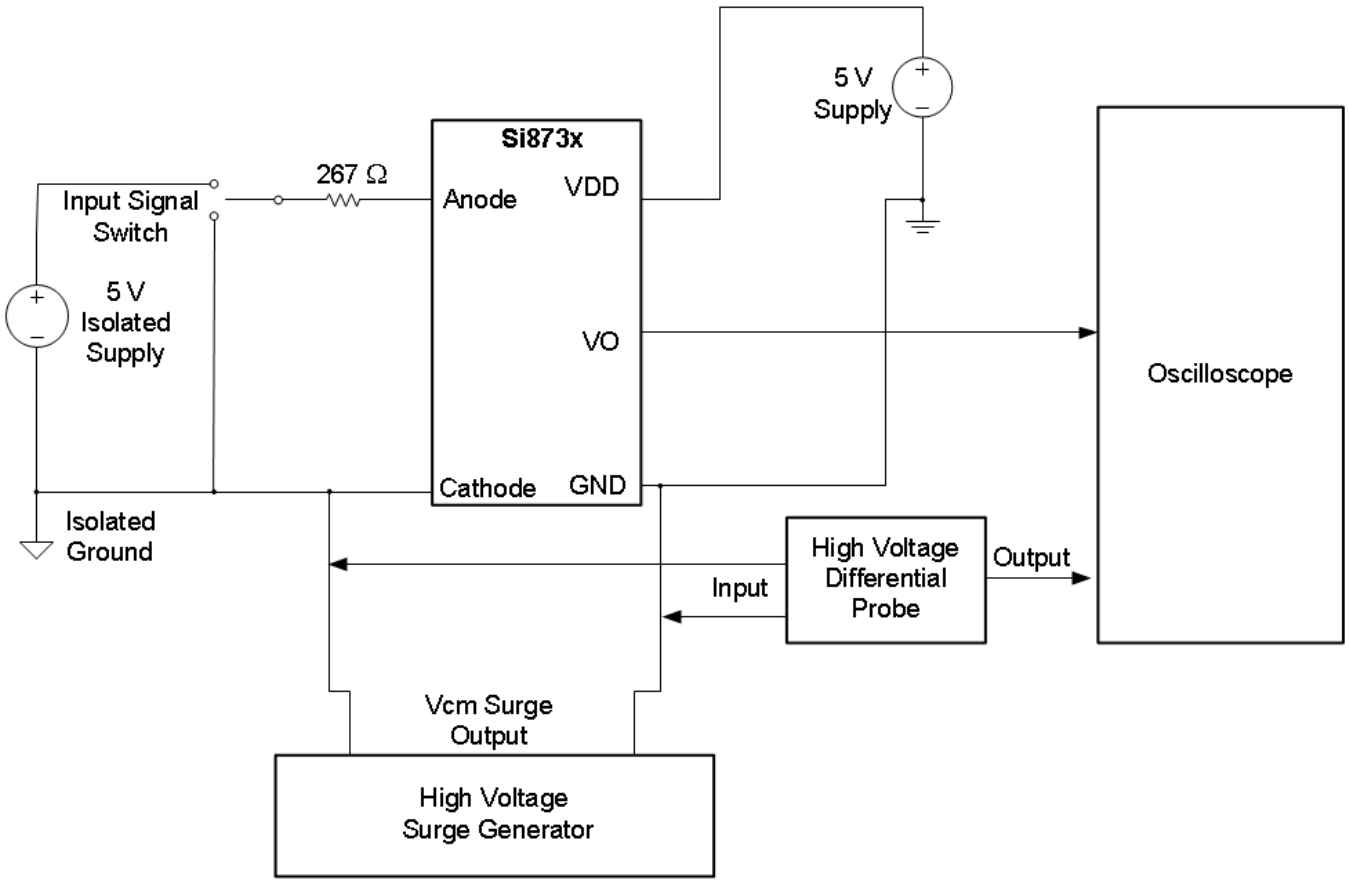


Figure 5.2. Common Mode Transient Immunity Characterization Circuit

Table 5.3. Regulatory Information

CSA (Pending)
The Si873x is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.
VDE
The Si873x is certified according to VDE0884. For more details, see File 5006301-4880-0001.
VDE0884-10: Up to 630 V_{peak} for reinforced insulation working voltage.
UL (Pending)
The Si873x is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 2500 V_{RMS} isolation voltage for basic protection.
CQC (Pending)
The Si873x is certified under GB4943.1-2011. For more details, see certificate “pending” yet TBD.
Rated up to 130 V_{RMS} reinforced insulation working voltage; up to 600 V_{RMS} basic insulation working voltage.
Note: Regulatory Certifications apply to 2.5 kV_{RMS} rated devices which are production tested to 3.0 kV_{RMS} for 1 sec. For more information, see 1. Ordering Guide.

Table 5.4. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value SOIC-8	Unit
Nominal Air Gap (Clearance)	L(IO1)		4.7 min	mm
Nominal External Tracking (Creepage)	L(IO2)		3.9 min	mm
Minimum Internal Gap (Internal Clearance)			0.016	mm
Tracking Resistance (Proof Tracking Index)	PTI	IEC60112	600	V
Erosion Depth	ED		0.031	mm
Resistance (Input-Output)*	R_{IO}		10^{12}	Ω
Capacitance (Input-Output)*	C_{IO}	f = 1 MHz	1	pF

Note: To determine resistance and capacitance, the Si873x is converted into a 2-terminal device. Pins 1–4 are shorted together to form the first terminal, and pins 5–8 are shorted together to form the second terminal. The parameters are then measured between these two terminals.

Table 5.5. IEC 60664-1 (VDE 0884) Ratings

Parameter	Test Condition	Specification SOIC-8
Basic Isolation Group	Material Group	I
Installation Classification	Rated Mains Voltages < 150 V_{RMS}	I-IV
	Rated Mains Voltages < 300 V_{RMS}	I-IV
	Rated Mains Voltages < 450 V_{RMS}	I-III
	Rated Mains Voltages < 600 V_{RMS}	I-III
	Rated Mains Voltages < 1000 V_{RMS}	I-II

Table 5.6. IEC 60747-5-2 (VDE 0884-10) Insulation Characteristics

Parameter	Symbol	Test Condition	Characteristic SOIC-8	Unit
Maximum Working Insulation Voltage	V_{IORM}		630	V peak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	1181	V peak
Transient Overvoltage	V_{IOTM}	t = 60 sec	6000	V peak
Pollution Degree (DIN VDE 0110, Table 1)			2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	Ω

Note: This isolator is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The Si873x provides a climate classification of 40/125/21.

Table 5.7. IEC Safety Limiting Values

Parameter	Symbol	Test Condition	Max SOIC-8	Unit
Case Temperature	T_S		140	°C
Input Current	I_S	θ_{JA} = 110 °C/W (SOIC-8), V_F = 2.8 V, T_J = 140 °C, T_A = 25 °C	370	mA
Output Power	P_S		1	W
Maximum value allowed in the event of a failure; also see the thermal derating curve in Figures Figure 5.3 (SOIC-8) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per VDE0884-10 on page 14, Figure 2.1 Simplified Channel Diagram on page 4, and Figure 3.1 Si8736 Operating Behavior ($I_F > I_{F(MIN)}$ when $V_F > V_{F(MIN)}$) on page 5.				

Table 5.8. Thermal Characteristics

Parameter	Symbol	Typical SOIC-8	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	110	°C/W

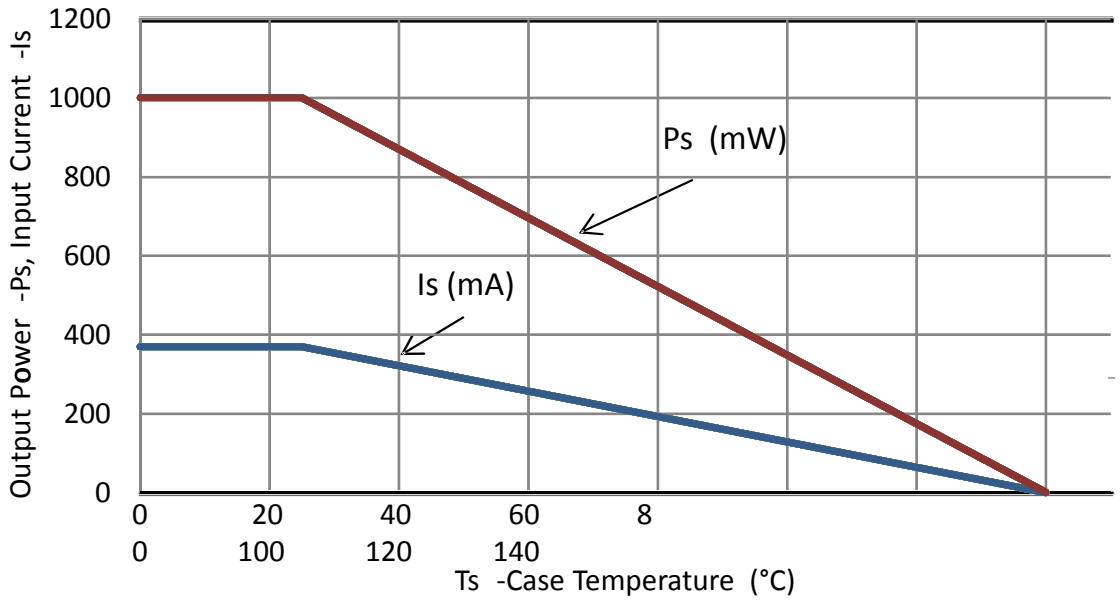


Figure 5.3. (SOIC-8) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per VDE0884-10

Table 5.9. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{STG}	–65	+150	°C
Operating Temperature	T_A	–40	+125	°C
Junction Temperature	T_J	—	+140	°C
Average Forward Input Current	$I_{F(AVG)}$	—	30	mA
Peak Transient Input Current (< 1 µs pulse width, 300 pps)	I_{FTR}	—	1	A
Reverse Input Voltage	V_R	—	0.3	V
Supply Voltage	V_{DD}	–0.5	7	V
Output Voltage	V_{OUT}	–0.5	V_{DD}+0.5	V
Enable Voltage	V_{EOUT}	–0.5	V_{DD}+0.5	V
Output Source or Sink Current	I_O	—	22	mA
Input Power Dissipation	P_I	—	90	mW
Output Power Dissipation	P_O	—	163	mW
Total Power Dissipation	P_T	—	253	mW
Lead Solder Temperature (10 s)		—	260	°C
HBM Rating ESD		3500	—	kV
Machine Model ESD		250	—	V
CDM		2000	—	kV
Maximum Isolation Voltage (1 s) SOIC-8		—	4500	V_{RMS}

Note: Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions specified in the operational sections of this data sheet.

6. Pin Descriptions (SOIC-8)

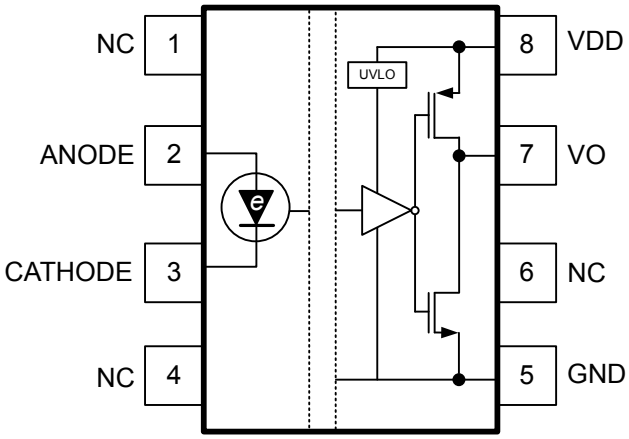


Figure 6.1. Pin Configuration

Table 6.1. Pin Descriptions (SOIC-8, DIP8)

Pin	Name	Description
1	NC*	No connect.
2	ANODE	Anode of LED emulator. V_O follows the signal applied to this input with respect to the CATHODE input.
3	CATHODE	Cathode of LED emulator. V_O follows the signal applied to ANODE with respect to this input.
4	NC*	No connect.
5	GND	Ground reference for V_{DD}. This terminal is typically connected to ground but may be tied to a negative or positive voltage.
6	NC*	No connect.
7	V_O	Output signal.
8	V_{DD}	Output-side power supply input referenced to GND (5.5 V max).
Note: No Connect. These pins are not internally connected. To maximize CMTI performance, these pins should be connected to the ground plane.		

7. Pin Descriptions (SOIC-8) with Output Enable

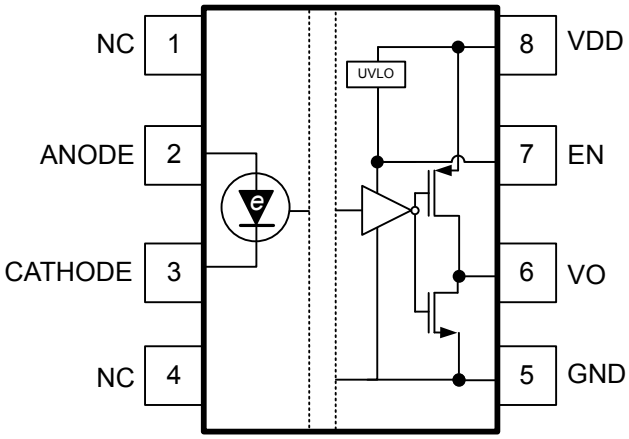


Figure 7.1. Pin Configuration

Table 7.1. Pin Descriptions (SOIC-8, DIP8) with Output Enable

Pin	Name	Description
1	NC*	No connect.
2	ANODE	Anode of LED emulator. V_O follows the signal applied to this input with respect to the CATHODE input.
3	CATHODE	Cathode of LED emulator. V_O follows the signal applied to ANODE with respect to this input.
4	NC*	No connect.
5	GND	Ground reference for V_{DD}. This terminal is typically connected to ground but may be tied to a negative or positive voltage.
6	V_O	Output signal.
7	EN	Output enable. Tied to V_{DD} to enable output.
8	V_{DD}	Output-side power supply input referenced to GND (5.5 V max).

Note: No Connect. These pins are not internally connected. To maximize CMTI performance, these pins should be connected to the ground plane.

8. Package Outline: 8-Pin Narrow Body SOIC

Figure 8.1 8-Pin Narrow Body SOIC Package on page 18 illustrates the package details for the Si873x in an 8-pin narrow-body SOIC package. Table 8.1 8-Pin Narrow Body SOIC Package Diagram Dimensions on page 18 lists the values for the dimensions shown in the illustration.

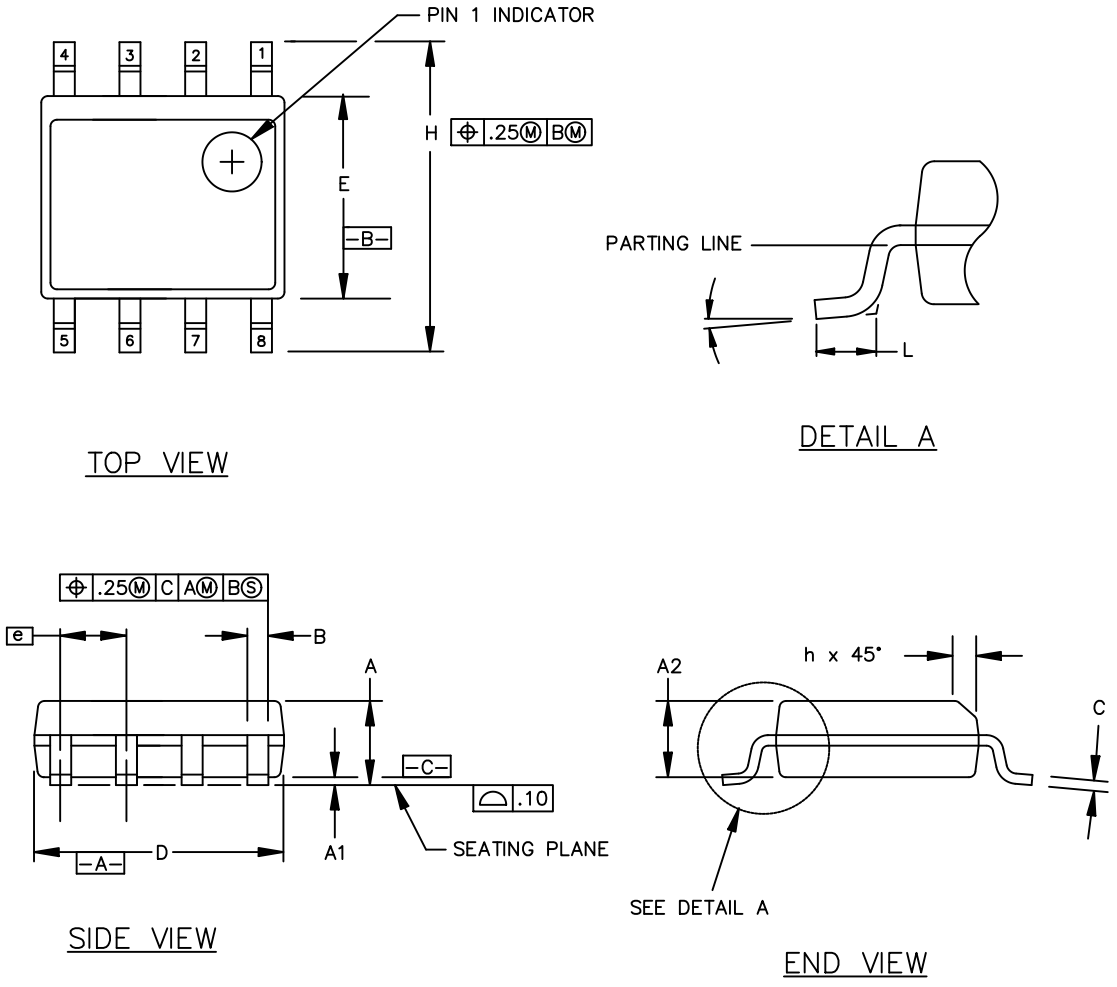


Figure 8.1. 8-Pin Narrow Body SOIC Package

Table 8.1. 8-Pin Narrow Body SOIC Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.40 REF	1.55 REF
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00

Symbol	Millimeters	
	Min	Max
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
	0°	8°

9. Land Pattern: 8-Pin Narrow Body SOIC

The figure below illustrates the recommended land pattern details for the Si873x in an 8-pin narrow-body SOIC. The table below lists the values for the dimensions shown in the illustration.

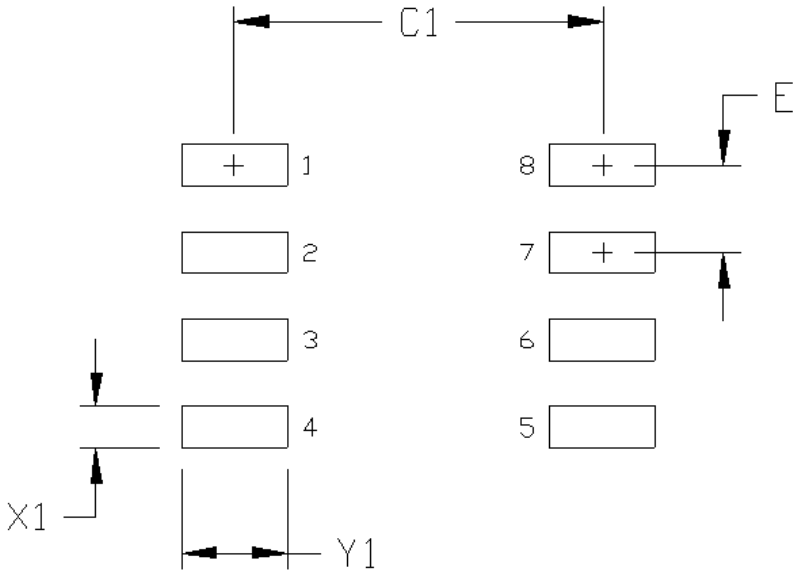


Figure 9.1. 8-Pin Narrow Body SOIC Land Pattern

Table 9.1. 8-Pin Narrow Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

10. Top Markings

10.1 Top Marking: 8-Pin Narrow Body SOIC

The figure below illustrates the top markings for the Si873x in an SOIC8 package. The table explains the top marks shown in the illustration.

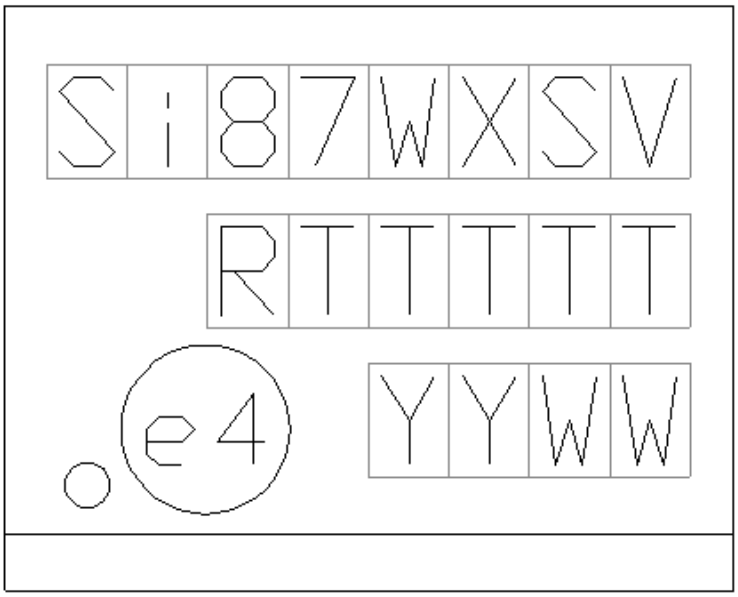


Table 10.1. SOIC8 Top Marking Explanation

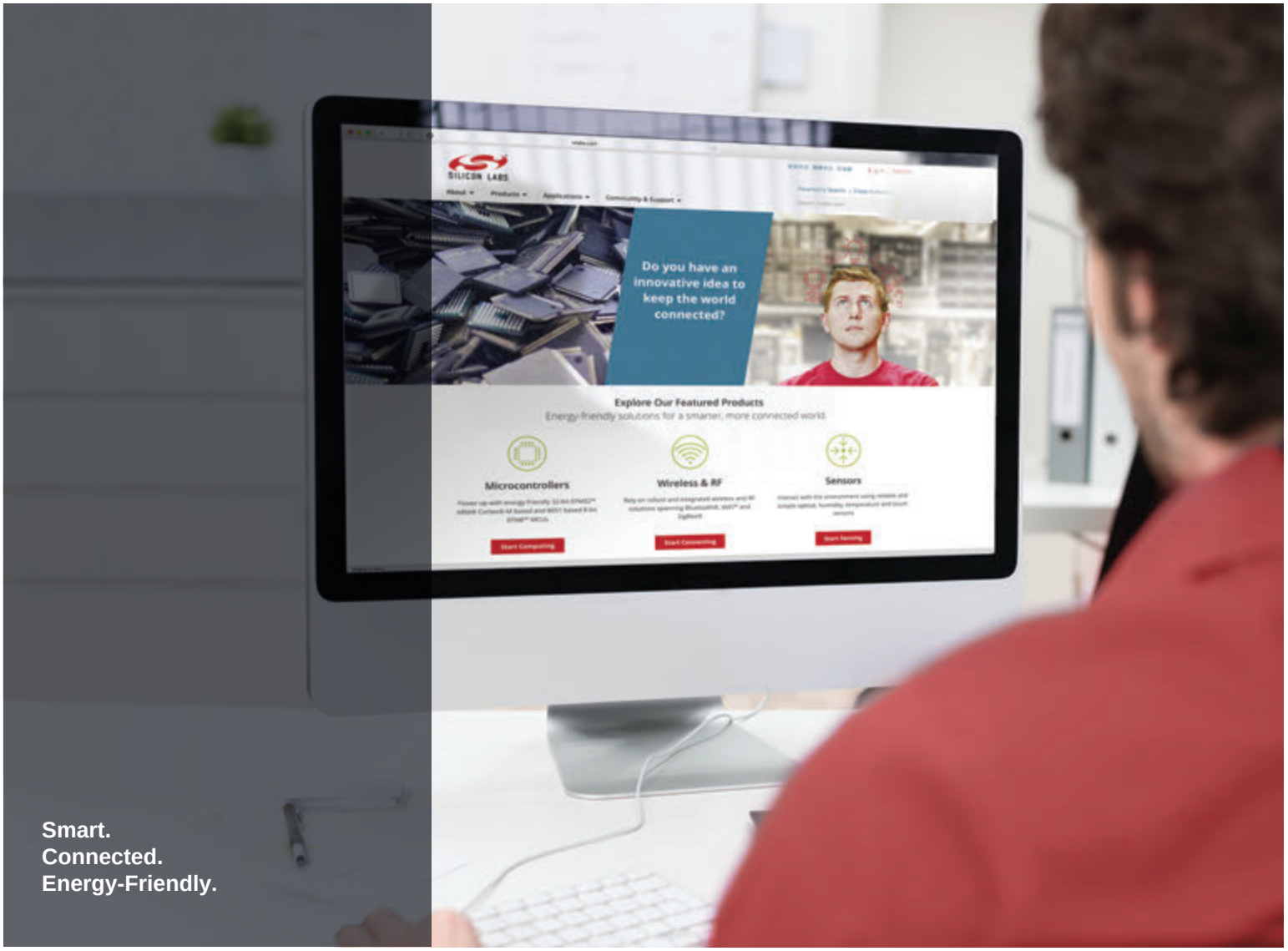
Line 1 Marking:	Customer Part Number	Si87 = Base name of product series W = Isolator product series (1 or 2) X = Output configuration 5/9 = no enable 6 = enable, output high when active 7/8 = enable, output Hi-z when active 0 = enable, output low when active S = Performance Grade: A = 15 Mbps, 20 kV/µs minimum CMTI B = 15 Mbps, 35 kV/µs minimum CMTI V = Insulation rating C = 3.75 kV
Line 2 Marking:	RTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form. “R” indicates revision.
Line 3 Marking:	Circle = 43 mils Diameter Left-Justified	“e4” Pb-Free Symbol
	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.

11. Revision History

Revision 1.0

March, 2018

- Initial revision.



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