IPDiA’s interposer solutions to various applications packaging and system miniaturization

December 2013
Outline

• Who is IPDIA?

• What is an Integrated Passive Device (IPD)? Main characteristics

• What is an Interposer? Main characteristics

• Why Interposer with IPD is key for miniaturization?

Examples in various applications
Who is IPDiA?
Who are we?

• Independent Company located in Caen, Normandy, France
• Dedicated to manufacturing of leading edge Integrated Passive Devices
• Operating its own Silicon wafer fab
• Strong R&D team and collaborations with leading research institutes
IPDiA: Turnkey Supplier

«One-Stop» Shop for the Integrated Passive Devices

From your schematics, we design and manufacture
High Quality Products
Industrial partner

**IPDIA manufactures** Semiconductor based products and is organized to support Med Tech companies.

- ISO-9001
- ISO-14001
- ISO-TS16949 (Automotive)
- ISO-13485 (Medical)
- OHSAS-18001
- RoHS compliant
Product for Performiniaturization

(1) Performiniaturization: process of miniaturizing and optimizing the performances of electronic boards
What is an IPD?

Main Characteristics
3D silicon passive devices with outstanding performances

**Capacitors**
- Superior temperature stability ($< 20$ppm / deg.C)
  - Technology characterized up to $+250^\circ$C
- Very low leakage current ($<40$pA)
- Superior DC voltage stability ($<0.1\%$/V)
  - No capacitance change over voltage variation.
- Very low ESR $< 15$mOhm
- Very low ESL $< 10$pH
- Negligible aging ($<0.001\%$ / 1000 hours)
- Excellent matching ($< 1.5\%$)
- Tolerance: 5%, 15%

**Coils**
- Superior Q-factor ($> 80$)
- Self-res. freq. $> 45$GHz
- Excellent matching ($< 1\%$)
- Tolerance: 5%, 15%

**Resistors**
- Excellent matching ($< 0.2\%$)
- Tolerance: 5%, 15%

**Zener Diodes**
- $BV>8V @1mA$ and ESD Capability 15KV Air discharge (IEC 61000-4-2, level4)

**Pin Diodes**
- Isolation $> 20$dB @500MHz
Key features of highly integrated capacitors

• Increase the effective capacitor surface by etching 3D structures with high aspect ratio.

<table>
<thead>
<tr>
<th></th>
<th>PICS1</th>
<th>PICS2</th>
<th>PICS3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Density (nF/mm²)</td>
<td>20</td>
<td>80</td>
<td>250</td>
</tr>
<tr>
<td>Depth (µm)</td>
<td>17</td>
<td>30</td>
<td>&gt;45</td>
</tr>
</tbody>
</table>

• Suitable high-k & low-k material
  – High permittivity
  – High breakdown voltage > 10V
  – Low leakage current <1nA
  – Excellent temperature and voltage linearity <100ppm/K & <100ppm/V
  – High reliability
Capacitor integration densities

- PICS5 1µF/mm²
- PICS4 500nF/mm²
- PICS3 250nF/mm²
- PICS2 80nF/mm²
- PICS1 25nF/mm²
- PICS 2DCS 2D-Connecting Substrate

Unique technology tailored to Digital ASIC needs
High performance technology optimized for both RF & Digital ASIC
High value technology optimized for RF ASIC
High performance technology optimized for RF baluns and filtering

Qualified for volume manufacturing
Under qualification
Under development
What is an Interposer?

Main Characteristics
General 2D-Interposer Platform

Interposers only

Interposers with IPD

Interposer + passive devices

PICS IPD
General 2.5D-Interposer Platform

Interposers only

Interposers with IPD
2D & 2.5D Interposer Platform

• Active components to be mounted onto the PICS interposer
  – Silicon die (Digital IC’s, Analog IC’s, low power discrete)
  – Small packages (Passive SMD, Oscillators, Diodes, Transistors, etc…)

• Interconnection processes : Wafer level package C2W
  – CoB technology: glue, die pick & place, wire-bond, dam&fill
  – Flip-Chip technol : flip-chip and underfill
  – packages pick & place : solder print, pick&place, reflow

• Silicon die to be reported : main characteristics
  – Die size : 250µm x 250µm up to 15mmx15mm
  – Die thickness : 80µm min
  – Pad size / pitch min : 40µm / 60µm
  – Aluminum based end-metal
## Advantages of Silicon as Interposer

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Printed Circuit Board (PCB)</th>
<th>Thick/thin flex</th>
<th>Ceramic</th>
<th>Silicon Interposer</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Line width / Spacing</strong></td>
<td>90µm down to 65µm for advanced PCB technologies</td>
<td>75µm down to 50µm for advanced thin flex technologies</td>
<td>75 µm to 50µm for advanced LTCC technologies</td>
<td>5µm</td>
</tr>
<tr>
<td></td>
<td>Accuracy around 25µm</td>
<td>Accuracy around 15µm</td>
<td>Accuracy around 15µm or less for LTCC</td>
<td>Below 1µm</td>
</tr>
<tr>
<td><strong>Metal layers for signal and routing management</strong></td>
<td>One metal layer in-between 2 thick laminated layer</td>
<td>Two layers for advanced flex technology</td>
<td>One layer</td>
<td>No limitation (2 to 3 layer)</td>
</tr>
<tr>
<td><strong>Via diameter</strong></td>
<td>200µm or below for advanced PCB</td>
<td>150µm for the best in class</td>
<td>120µm for advanced LTCC</td>
<td>75µm or below</td>
</tr>
</tbody>
</table>

Comparison on main dimensions aspects
### Advantages of Silicon as Interposer

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Printed Circuit Board (PCB)</th>
<th>Thick flex</th>
<th>Ceramic</th>
<th>Silicon Interposer</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTE1</td>
<td>~ 20 ppm/°K</td>
<td>~ 20 ppm/°K</td>
<td>~ 10 ppm/°K</td>
<td>~ 2 ppm/°C</td>
</tr>
<tr>
<td></td>
<td>Big CTE mismatch with DSP and memories die set</td>
<td>Big CTE mismatch with DSP and memories die set</td>
<td>Slight CTE mismatch with DSP and memories die set</td>
<td>No CTE mismatch with DSP and memories die set</td>
</tr>
<tr>
<td>Temperature</td>
<td>Limited to 250°C with warpage</td>
<td>Lower than 200°C with polymer degradation</td>
<td>Higher than 400°C For HTTC</td>
<td>Higher than 400°C</td>
</tr>
<tr>
<td>Packaging Process compatibility</td>
<td>Very good with SMD</td>
<td>Good with SMD</td>
<td>Good with SMD</td>
<td>Good with SMD</td>
</tr>
<tr>
<td></td>
<td>Specific adjustment with silicon die set</td>
<td>Good with silicon die set</td>
<td>Specific adjustment with silicon die set</td>
<td>Very good with silicon die set</td>
</tr>
</tbody>
</table>

Comparison on main thermal, thermo-mechanical and material aspects
**Through Silicon Vias: Highlights**
- Low power consumption
- Short connection
- High density
- Good heat dissipation
- Reduced RC delays
- Low resistivity
- Smallest area
- High routing density

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**TSV coupled with IPD**
Typical cross-sectional view of a PICS IPD with integrated Through Silicon Vias

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**Through Silicon Vias coupled with IPD Technology (PICS): Applications**
- Interposer with System in Package (SiP)
- Wafer Level Package (WLP), attachable directly on PCB
- Interposer for submount / carrier
- Die stacking for volume constrained applications
TSV Basic Tool Boxes

- Deep Silicon Etch
- Isolation and Barrier Layer deposition
- 3D Lithography
- Copper Electroplating in vias
- Double side Patterning and thin wafer manipulation
- Passivation and Ni-Au finition
# Electrical performances

<table>
<thead>
<tr>
<th>Designation</th>
<th>Value</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die thickness</td>
<td>200 μm typ</td>
<td></td>
</tr>
<tr>
<td>Via diameter</td>
<td>75 μm</td>
<td></td>
</tr>
<tr>
<td>Via pitch</td>
<td>125 μm</td>
<td></td>
</tr>
<tr>
<td>Via density</td>
<td>Max 64 Vias/mm²</td>
<td></td>
</tr>
<tr>
<td>Via filling</td>
<td>Copper</td>
<td></td>
</tr>
<tr>
<td>Max allowed current per via</td>
<td>100mA</td>
<td>Limited by the measurement equipment</td>
</tr>
<tr>
<td>Isolation breakdown voltage</td>
<td>&gt; 200V</td>
<td></td>
</tr>
<tr>
<td>Serial resistivity per via</td>
<td>&lt; 10 mOhms</td>
<td>See curve for details &lt; 10mOhms up to 5GHz</td>
</tr>
<tr>
<td>Serial inductor per via</td>
<td>&lt; 100pH</td>
<td>See curve for details ~50pH up to 10GHz</td>
</tr>
<tr>
<td>Via-bulk isolation</td>
<td>&lt; 1pF</td>
<td></td>
</tr>
<tr>
<td>IPD generation</td>
<td>PICS2C</td>
<td>Passive components such as high-density trench capacitors (80nF/mm²), MIM capacitors (80pF/mm²), resistors, and high-Q Cu inductor.</td>
</tr>
</tbody>
</table>

Series resistors and parasitic Inductors of vias versus frequency:

Results on through silicon vias with a 75μm diameter and a 300μm depth
• Typical TSV’s RLC (20 GHz)
  - Rs < 0.5 Ohm
  - Ls < 400fH
  - Cs < 200 fF
  - G (isolation) < 4.10e-4 S (R > 2.5KOhm)

• Typical TSV’s R en DC
  - R < 60 mOhm

• 1dB attenuation on transmission freq ~ 20Ghz (GND on 1st neighboring via)

• >20db isolation VIA to 1st neighboring VIA @ 20Ghz
## Interposer with TSV: main design rules

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>SPECIFICATIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interposer Thickness (Without Via)</td>
<td>[100 µm ; 400 µm]</td>
</tr>
<tr>
<td>Interposer Thickness (With Via)</td>
<td>300 µm standard</td>
</tr>
<tr>
<td>TSV diameter</td>
<td>75 µm (Copper)</td>
</tr>
<tr>
<td>Vias filling</td>
<td>Copper or Non metal</td>
</tr>
<tr>
<td>Barrier layer</td>
<td>Optional</td>
</tr>
<tr>
<td>Finition 0</td>
<td>Optional</td>
</tr>
<tr>
<td>Finition 1</td>
<td>Optional</td>
</tr>
<tr>
<td>Via minimum pitch</td>
<td>125 µm</td>
</tr>
<tr>
<td>Layer 0 metal thickness</td>
<td>Copper 4 to 8 µm upon request</td>
</tr>
<tr>
<td>Layer 1 metal thickness</td>
<td>Aluminum 1µm</td>
</tr>
<tr>
<td>Layer 2 metal thickness</td>
<td>Copper 10 to 15 µm</td>
</tr>
<tr>
<td>Layer 0 metal minimum width</td>
<td>8 µm</td>
</tr>
<tr>
<td>Layer 1 metal minimum width</td>
<td>1.5 µm</td>
</tr>
<tr>
<td>Layer 2 metal minimum width</td>
<td>8 µm</td>
</tr>
<tr>
<td>Minimum space between 2 metal lines (Layer 0)</td>
<td>8µm</td>
</tr>
<tr>
<td>Minimum space between 2 metal lines (Layer 1)</td>
<td>4 µm</td>
</tr>
<tr>
<td>Minimum space between 2 metal lines (Layer 2)</td>
<td>6 µm</td>
</tr>
</tbody>
</table>
More important added values has to be understood as an exponential benefit raised step by step from 2D to 2.5D with the following:

- **Miniaturization (Volume reduction)**
- **Power consumption reduction (Metal track / Passive Integration)**
- **RF performances (Connection length and passive integration technology)**

Replacement of external Passive (PICS benefit):

- Footprint reduction & volume reduction compared to external
- Added performances thanks to integrated passive technology
- Surface and performances thanks to silicon routing design rules

External component integration (2D interposer benefit – vertical one side):

- External components integration (System generation)
- Both packages and die could be integrated (Mixed technology)
- Semiconductor design rule compatibility (Material, downsizing)
- Component placement and spacing reduction

External component integration (2.5D interposer benefit – vertical 2 sides):

Same as 2D, with TSV (Through silicon vias):

- Both side external component integration (Mixed technology – 2 sides)
- Footprint reduction (Vertical interconnection of the module to the customer applicative substrate)
Interposer Key Value for Miniaturization Examples in Various Application
**Application**: Medical sensor module including RF communication suitable for Defibrillation

**Description**: 2D interposer with passives integration suitable for external ICs and package platform, put onto an applicative PCB

**Interposer value as seen by the customer**
- Very stable high capacitor integration
- Miniaturization using IPD and 2D packaging
- Stable Flip-Chip technology
- Decreasing total system weight (Equipment)
- Silicon-Silicon compatibility for 3D packaging (Reliability)
RF Module for defibrillator

Complete RF Module

- RF Transceiver
- XO
- SAW Filter
- 400MHz & 2.4GHz Matching network with integrated coils
- Decoupling capacitances

Using PICS technology:

→ 40% area decrease!
→ 25% height decrease!

SMD & PCB technologies

2D interposer with PICS technology

- 112 mm² / 1.6mm height
- 72 mm² / 1.2mm height

-35% on used surface
Example of Miniaturization in Implantable Devices

The smallest Pacemaker

Today ➔ 10 cm³

2014 ➔ 1 cm³
2D-interposer with PICS for Base station

**Application**: 2D interposer suitable for Base station high integration density package

**Description**: 2D interposers with passives integration suitable for external IC and package platform, put onto an applicative PCB

**2D Interposers with IPD + 3D packaging**

**Interposer value as seen by the customer**

→ Integration (Miniaturization using IPD and 3D packaging)
→ 3 x 2D-interposer platforms with IPD
→ Silicon-Silicon compatibility for 3D packaging (Reliability)
2.5D interposer for wafer test

Application: Interposer suitable for Wafer Test Equipment

Description: Interposer is used as a space transformer between complex IC (> 2500 i/o’s, 45µm pitch) and PCB dimension (150µm pitch). TSV 3D-interconnexion from top to bottom

Interposer value as seen by the customer
- Routing density capability on top not possible with other interposers (Ceramic or flex)
- High level 3D interconnexion density (TSV)
- Silicon-Silicon compatibility for 3D packaging (Solderable flip-chip)
2.5D interposer for high value captor

Application: 3D packaging suitable for high level Particle Detection

Description: TSV post processing on customer ASIC + 3D packaging technology (Detector die flipped onto ASIC-TSV, both flipped over PCB)

Interposer value as seen by the customer
→ Increasing pixel coverage by flip-chip and TSV
→ Decreasing total system weight (Materials)
→ 3D interconnection density (TSV) capability
→ Silicon-Silicon compatibility for 3D packaging (Solderable flip-chip)
2.5D interposer with PICS for aerospace

**Application**: 3D packaging suitable for motor control in aerospace domain

**Description**: IPD with TSV 2.5D-interposer + 3D packaging technology (Number of stacked die in CoB and discrete package in SMT)

**Interposers + IPD + 3D packaging**

**Interposer value as seen by the customer**
- Integration and miniaturization using Passive Integration, TSV and 3D packing
- Stack die technology on 2.5D interposer
- Decreasing total weight of the component
- 3D interconnxion density (TSV) capability
- Silicon-Silicon compatibility for 3D packaging (Reliability)
Conclusion
2D & 2.5D Interposer with IPD benefits

- Integration of passive component: PICS (Wafer processing)
  - adapted Passive and ESD diodes network integration
  - system miniaturization thanks to passive & interconnection form factor

- External components integration: Interposer (Packaging processing)
  - External IC’s and packages picked & placed (CoB) or flipped
  - Optimum Interconnection form factor thanks to wafer processing form factor

- To interconnect integrated passives & external components (2D-interposer)
- To interconnect top and bottom sides (3D-interposer)

- Increased miniaturization of your electronics

- Improved reliability thanks to very low ageing and reduced number of passive components

- Enhanced performances thanks to the high stability of silicon capacitors

- Improved battery operations because of very low-level leakage currents in IPD devices, and metal track design on silicon
IPDiA’s solutions can help to decrease volume & size of your electronics and improve their reliability